Instrumentation of a high-sensitivity microwave vector detection system for low-temperature applications

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We present the design and the circuit details of a high-sensitivity microwave vector detection system, which is aiming to study the low-dimensional electron system embedded in the slots of a coplanar waveguide at low temperatures. The coplanar waveguide sample is placed inside a phase-locked loop; the phase change of the sample may cause a corresponding change in the operation frequency, which can be measured precisely. We also employ a double-pulse modulation on the microwave signals, which comprises a fast pulse modulation for gated averaging and a slow pulse modulation for lock-in detection. In measurements on real samples at low temperatures, this system provides much better resolutions in both amplitude and phase than most of the conventional vector analyzers at power levels below -65 dBm in the frequency range from 100 MHz to 18 GHz. © 2005 American Institute of Physics. [DOI: 10.1063/1.2006327]

I. INTRODUCTION

In the study of dynamic magnetotransport behaviors of low-dimensional electron systems (LDESs), such as two-dimensional electron systems (2DESs),¹⁻⁵ quantum wires (QWs),⁶ and anti quantum dots (QDs),⁷ a microwave vector detection system, which can measure both the amplitude and the phase variations of the signals under the influence of the LDESs in magnetic fields, is indispensable. Usually people use a conventional vector network analyzer (VNA) as such a detection system by virtue of its expediency and broadband characteristics. The LDES under test can be either embedded in the slots of a coplanar waveguide (CPW),^{1-5,7} attached to a resonator,⁸ or directly connected to a coaxial cable;⁹ then the transmission or reflection property can be measured, and the transport properties of the LDES can be extracted therefrom, as the external magnetic field (B), or the temperature (T) changes. However, since in most of these studies the LDES is placed in a very cold environment with temperature (T) below 4.2 K, or even down to several tens of millikelvins, the power of the excitation signal must be very low, normally below -60 dBm, to avoid joule heating. Moreover, the power reaching the detection system is even lower due to the loss of coaxial cables and the sample itself. Hence the resolution of the data, in particular the phase part, becomes very poor.

In this article, we present the instrumentation and the details of circuit design of a very-high-sensitivity vector detection system,¹⁰ incorporating phase-locked loop (PLL) and double pulse techniques. Here we mainly emphasize the ap-

plication of this system to the study of LDESs embedded in the slots of a CPW, which have been successfully used as broadband sensors.^{1-5,7} Our method is especially useful for the case of QDs or QWs, whose relatively small effective area compared to 2DES samples usually results in a very small variation on the transmission coefficient of the CPW sample, and makes the conventional VNA measurement very formidable and impractical.

In a typical modern VNA, a PLL is only used in the very front end of its superheterodyne receiver¹¹ to make the local oscillator (LO) of the first-stage mixers follow the reference signal from the tracking source, and thus to preserve the phase information in the detected signal. In contrast, we put the CPW sample under test in the high-frequency signal path of a PLL, which is renowned for its phase sensitivity, and obtain a great improvement in the phase resolution. As a matter of fact, the PLL-based phase detection technique has been applied in the study of 2DESs using surface acoustic wave (SAW).¹² We improve the design of their measurement system, including a better pulse averaging part, a homodyne amplitude detection part, and a loop filter of the PLL, and also replace the SAW transducers with a coaxial cable delay line and a broadband CPW containing a LDES under test. All these result in a very sensitive microwave vector detection system, which can be operated with extremely low power levels through samples, making this system very suitable for low-temperature applications.

This system has been used to study the dynamic magnetotransport properties of a QW-array embedded in a CPW¹⁰ with an average power below -65 dBm into the sample at 0.3 K, and the resolution of the data, including both the amplitude and phase variations, surpassed what most of the commercial VNAs can get at such a low power level. We

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FIG. 1. (Color online) Simplified schematic diagram of the vector detection system. The meandering CPW containing a LDES in the gaps is part of the microwave signal path in the PLL.

have also used this method to obtain very clean data of the high-frequency longitudinal conductivity, including both the real and the imaginary parts, of a 2DES in the quantum Hall plateau.

II. SYSTEM AND CIRCUIT DESIGNS

A. Phase measurement with a PLL

The principle of phase detection by a PLL¹³ is quite straightforward. Two semirigid coaxial cables of total length L connect the PLL and the CPW sample. The PLL can tune its operation frequency (f) to ensure the sum ($\Delta\phi$) of the phase change of the semirigid cables ($\Delta\phi_L$) and the CPW sample ($\Delta\phi_s$) is 0, i.e., $\Delta\phi = \Delta\phi_L + \Delta\phi_s = 0$, or $\Delta\phi_s = -\Delta\phi_L$. Here $\Delta\phi_L$ can be easily obtained from $\Delta\omega\tau_L$ or $2\pi\Delta fL/v_L$, where ω is the angular frequency ($2\pi f$), v_L the phase velocity of the signal in the cable, and τ_L the delay time of the coaxial cable. Thereby we can obtain $\Delta\phi_s$ directly from measuring the frequency change (Δf) of the PLL via

$$\Delta\phi_s = -\Delta\phi_L = -2\pi\Delta fL/v_L = -\Delta\omega\tau_L. \quad (1)$$

B. Description of the complete system

Figure 1 shows the complete schematic diagram of the detection system, consisting of the pulse handling part, the microwave PLL, and the amplitude readout part, together with the CPW sample in a cryogenic environment. The main microwave components of this system are basically a pair of homodyne mixers (M1 and M2) with different reference signals of quadrature phase difference generated by a 90° hybrid (H). The signal from the sample is divided equally into two parts by a power divider (D). The mixer M1 with a 0° reference (LO1), used as the phase sensitive detector (PSD), has zero output (IF1) forced by the PLL, and at the same

FIG. 2. Time sequence of the controlling, sampling, and some output pulses. The time scale in (b) is much shorter than (a).

time the other mixer M2 with a 90° reference (LO2) has an output (IF2) proportional to the amplitude of the signal.

To reduce the signal power level and increase the signal to noise ratio, besides homodyne detection we also employ a double-pulse modulation scheme to detect and average the microwave signal. Figure 2 shows the sequence of the controlling pulses and some other related outputs. A short pulse train [GP in Fig. 2(b)] with a 0.2–2 μs pulse width and a 0.1%–10% duty cycle, provided by a pulse generator (PG in Fig. 1) and gated by a slow square-wave TTL signal (TTL1) shown in Fig. 2(a) with a period of 1–10 ms from a lock-in amplifier, modulates the microwave signal sent to the sample. A time-delayed pulse (SP) with a 0.2–1 μs pulse width, triggered by the modulating pulses, controls a sample-and-hold (SH) circuit that samples the IF output (IFO) of the microwave mixer. The output of the SH circuit (SHO) is set to zero by an analog switch when the TTL gating signal is low. The output of the SH circuit has the same characteristic frequency as the signal TTL1, and hence can be averaged and read out by the lock-in amplifier.

We use two sets of pulse averaging circuits in this system, one for the PLL part and the other for the amplitude detection part. Even though the lock-in amplifiers therein are synchronized at the same operating frequency, their averaging time constants are different. The time constant of LOCKIN1 in the PLL is about 1–10 ms for fast loop dynamics, in contrast to 300 ms or 1 s of LOCKIN2 in the amplitude readout part for low average noise. The average of the PSD output (IF1) is then sent to an integrator (loop filter of PLL), whose output is connected to the frequency modulation (FM) input of the microwave source (SG), i.e., the VCO of the PLL, and thus the loop is closed.

C. Pulse handling circuits and the integrator

The short pulse trains used in this system are provided by a simple single-channel pulse generator TPG110 from

FIG. 3. Simple pulse shaping circuit to generate a 0.2–2 μ s pulse from a 30 ns input pulse.

TTi,¹⁴ which can generate a short reference pulse train (SYN in Fig. 2) and a pulse train (SP) with tunable time delay (relative to SYN), pulse width, and duty cycle, and a home-made pulse shaping circuit (Fig. 3), which converts the 30-ns-width reference pulses (SYN) to the gating pulses (GP) with 0.2–2 μ s pulse width (adjustable by R1, R2, and R3) that are sent to a diode switch (S) to modulate the microwave signal. A lock-in amplifier (LOCKIN1), SR830 from SRS,¹⁵ sends a slow TTL square-wave reference (TTL1) to the “trigger/gate in” input of TPG110. Another lock-in amplifier (LOCKIN2) is externally locked to LOCKIN1 and used to read the IF output of M2 (IF2).

Each IF output of the mixers (M1 and M2) is low-pass filtered and then amplified by a pulse amplifier before being fed into the sample-and-hold circuit. The low-pass filters used here are PLP-5 ($f_{3\text{ dB}}=5$ MHz) or PLP-70 ($f_{3\text{ dB}}=70$ MHz) from Mini-Circuits,¹⁶ depending on the pulse width of the gating pulse (GP). For the pulse amplifier, we use a high-speed low-noise operational amplifier MAX4107¹⁷ connected in a noninverted configuration as shown in Fig. 4. Its rise/fall time is well below 10 ns for a typical pulse height (≤ 1 V) in our application.

The sample-and-hold circuit is shown in Fig. 5. We use a high-speed sample-and-hold amplifier IC HA-5320-5,¹⁸ and a fast analog switch ADG201HS¹⁹ followed by a buffer BUF04.¹⁹ The main output of TPG110 (SP) is connected to the S/H control (lead 14) of HA-5320-5, and the slow reference TTL1 from LOCKIN1 controls ADG201HS and makes the output SHO zero as TTL1 goes low.²⁰

A simple integrator shown in Fig. 6 serves as the loop filter of the PLL. The integration time constant (R_4C_2) is about 23 ms, which is chosen to be higher than the time constant of LOCKIN1 such that the dynamics of the PLL is

FIG. 4. Circuit of a pulse amplifier.

FIG. 5. (a) Sample-and-hold circuit with (b) an analog switch and a buffered output.

mainly controlled by this integrator. R5 gives the PLL an adequate damping that may attenuate unwanted oscillations in the loop. The dynamic properties of this PLL system will be discussed later in Sec. III.

D. Microwave modules

We use several sets of microwave modules to cover the frequency range from about 100 MHz to 18 GHz. Table I lists the model numbers of the modules (including the vendors in Ref. 21) according to their operation band. Please note that the amplifiers (A) includes a front-end low-noise preamplifier (LNA) and subsequent amplifiers to make the total gain about 60 dB. To cover the whole band, we use two LNAs with noise figure (NF) better than 1.4 and 2.2 dB for frequency range 0.1–8 and 6–18 GHz, respectively. The microwave signal source (SG) used here is model E4421B (250k–3 GHz) or E8254A (250k–40 GHz) from Agilent,²¹

FIG. 6. Circuit of the integrator (loop filter) in the phase-lock loop.

TABLE I. The model numbers of the microwave modules.

Band (GHz)	Diode switch (S)	Mixer		Divider (O)	LNA+ Amp(A)	Directional coupler (C)
		(M1 and M2)	90° hybrid (H)			
0.1–0.5	ZASWA-2-50DR ^a	ZFM-2000 ^a	QE-18-E ^c	ZFSC-2-2500 ^a	AFS3-00100800-14-10P-4 ^b +ZJL-7G ^a ×3	ZFDC-20-5 ^a
0.4–2			QS4-01-464/6 ^c			(−19.5±0.5dB) ^a
2–4.3	ZASWA-2-50DR ^a	ZEM-4300 ^a	QS4-01-464/3 ^c	ZFSC-2-10G ^a	AFS3-00100800-14-10P-4 ^b +ZJL-7G ^a ×3	86205A ^f (−16.5 dB)
4–7	138BDF1 ^b	DB0218LW2 ^b	QS2-07-464/4 ^c	2089-6209-00 ^d	AFS3-00100800-14-10P-4 ^b +ZJL-7G ^a ×3	87300B ^f
6–18					AFS5-06001800-22-10P-6 ^c +QLW-12124033 ^d	(−16 dB)

^aMini-circuits.^bMITEQ.^cQuinstar.^dM/A COM.^ePulsar microwave.^fAgilent.

both with FM bandwidth down to dc and oven-stabilized time base. The phase noise of the SG is well below -70 and -110 dBc/Hz at 10 Hz and 20 kHz deviations, respectively; the influence of the phase noise can be further reduced by proper averaging processes.

III. RESULTS AND DISCUSSIONS

A. Response of the PLL

The response of this PLL system is mainly controlled by four parameters, the power of the signal from the sample back to the LNA, the sensitivity of LOCKIN1 (V_{sen}), the FM deviation per volt (F_{FM} , with unit Hz/V) of the VCO, and the total length of the semirigid coaxial cables, all of which can be tuned by the instrumental setting in our design. The length of the semirigid cables affects the delay time τ_L in Eq. (1). We can measure τ_L precisely with this PLL system itself without using an additional conventional VNA or time domain reflectometer. In the unlock condition, i.e., with FM off in SG (VCO), we recorded the output of LOCKIN1 (or LOCKIN2) as a function of frequency f , and the result can be expressed as $A_{ul} \exp(2\pi f \tau_L + \varphi_0)$ with A_{ul} the oscillation amplitude, and φ_0 a relative phase factor. Figure 7(a) shows the oscillations for both LOCKIN1 and LOCKIN2 near $f = 1.2$ GHz with only a 10.4 m semirigid cable and no sample connected to the PLL system between the attenuator (AT) and A in Fig. 1. As expected, the oscillations of these two channels are 90° out of phase due to the LO phase difference of two mixers. From the “frequency” of these oscillations, we can directly estimate τ_L to be 53.3 ns. Figure 7(b) shows that τ_L is a linear function of the length of the semirigid cable with a finite intercept, about 2.6 ns, on the vertical axis. This extra delay time corresponding to a zero-length cable can be attributed to the time delay in the microwave modules. The peak power of the microwave signals used in these tests is -70 dBm.

The phase change of the CPW device in the experiment is the product of the output of the integrator V_{FM} in the PLL, F_{FM} , and τ_L while keeping the PLL in the locked condition. $V_{\text{FM}} F_{\text{FM}}$ is in fact the change in the frequency (Δf) of the

VCO, which can also be measured by a microwave counter. F_{FM} of the signal source may affect the phase resolution: the smaller the FM deviation set, the higher is the phase sensitivity. However, if F_{FM} is set too small, the PLL may saturate very easily (the output of the integrator V_{FM} reaches $+1.4$ or -1.4 V), and the phase signal readout V_{FM} is also very noisy. Usually F_{FM} needs to be set properly according to the dynamic range of the phase signal.

For low-temperature experiments, usually the signal

FIG. 7. (Color online) (a) Output oscillations of LOCKIN1 and LOCKIN2 with only a 10.4 m semirigid cable and no sample connected to the PLL system. (b) Delay time τ_L vs length (L) of the semirigid cable.

FIG. 8. (Color online) Normalized step responses measured from the output of the integrator with different sensitivity levels of LOCKIN1.

power to the sample is set by a step attenuator and is chosen to be the highest value without any heating effect on the sample. For samples immersed in liquid He3 at 0.3 K, typically a peak power of -50 dBm microwave signal, equivalent to an average power of -65 to -80 dBm depending on the duty cycle of the modulating pulses, can be delivered to the sample without raising the sample temperature.

The response time of the PLL is affected by the total gain of the loop, which can be obtained from the amplitude of the oscillations in Fig. 7(a) and F_{FM} . A_{ul} can be easily controlled by V_{sen} of LOCKIN1, and this provides a very convenient method to control the response time of the PLL during the experiment. Figure 8 shows the step response for different value of V_{sen} . In this test, we also used a 10.4 m semirigid cable without sample attached to the PLL system. F_{FM} was set at 1 MHz/V, the peak power of the microwave signal after the attenuator was -70 dBm, and the operation frequency was about 1.2 GHz. The step response was measured from the output of the integrator V_{FM} as function of time right before we increased the unmodulated frequency of SG by a step of 500 kHz while the PLL was kept in a locked condition. The rise time of the response can be tuned from 0.63 s for $V_{\text{sen}}=1$ V to 0.015 s for $V_{\text{sen}}=50$ mV, and at the same time the loop dynamic behavior is moved from an overdamped regime to a slightly underdamped regime. We also find that the fluctuation of the signal decreases as V_{sen} increases. There is apparently a tradeoff between the speed of the loop and the signal fluctuation.

B. Detection limit

To gain an idea of the detection limit of this system, we measured the background noise in the phase signal with only a 5.4 m semirigid cable attached to the system. Various microwave modules were used to cover the whole available frequency range. Figure 9 shows the measured peak-to-peak phase fluctuation versus frequency for different peak power levels of the microwave signal after the step attenuator (AT) together with the loss of the semirigid cable measured by a VNA. The phase signal was read from V_{FM} and then multiplied by $F_{\text{FM}}\tau_L$. The measured bandwidth is controlled by the time constant of the integrator (23 ms), equivalent to about 7 Hz. V_{sen} was fixed at 500 mV and V_{FM} was set at 50 kHz/V during this test. The modulating pulses had a 2 μ s pulse

FIG. 9. (Color online) Background peak-to-peak noises in the phase signal as functions of frequency f tested with different power levels. The loss of a 5.4 m semirigid cable is also shown for comparison.

width and a 1/75 duty cycle. The gating window of the SH circuit was 350 ns.

The collected data shown in Fig. 9 indicate that below 5 GHz, even for the lowest peak power -90 dBm in our test, the phase fluctuation is still less than 0.0003° ; above 5 to 18 GHz, the fluctuation is still controlled within about 0.002° . This noise level is remarkably low for such a low-power signal. Here we want to note that to obtain the average power value we must further subtract about -21.8 dBm from the peak power value due to the low duty cycle. In fact, the signal power reaching the low-noise amplifier (LNA) is even lower than the input value claimed above due to the loss of the cable as also shown in Fig. 9. This may explain the noise in phase increases at high frequencies. The resolution with a low- T sample loaded is slightly worse due to the loss of the sample and extra noise from the cryogenic environment. The resolution of the amplitude readout for a small-variation signal can be enhanced by the use of the “offset” and “expand” functions of the lock-in amplifier.¹⁵

C. Applications to low-dimensional electron systems

In the following we will present measured results for a 2DES sample (sample A) and a QW array sample (sample B) to demonstrate the capability of this system. The 2DES in sample A is confined in a 20-nm-wide modulation-doped $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ quantum well grown on GaAs substrate by molecular beam epitaxy technique. The quantum well is separated from a 260 nm $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ Si-doped layer by a 15 nm GaAs and a 5 nm $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ undoped spacer layers. This 2DES has an electron density of $5.95 \times 10^{11} \text{ cm}^{-2}$ and a mobility of about $3.2 \times 10^5 \text{ cm}^2/\text{V s}$ at 0.3 K. A 50 Ω (Z_0) meandering CPW made of Au(300 nm)/Ti(10 nm) with a 36- μm -wide central conductor and a 23 μm gap (d) between the central conductor and the ground plane at both sides is manufactured on the surface of the substrate. The effective length ℓ of the meandering CPW is 2.25 cm. The sample is immersed in liquid ^3He (0.3 K) with applied B

FIG. 10. (Color online) Measured $\text{Re}\{\sigma_{xx}\}$ and $\text{Im}\{\sigma_{xx}\}$ of a 2DES in an InGaAs quantum well embedded in the slots of a CPW at 0.3 K with the PLL operating at 6.99 GHz. The integer number with an arrow marks the Landau level filling factor at that field.

perpendicular to the sample surface. The real part and the imaginary part of the longitudinal conductivity can be deduced from the relative amplitude change¹ of the microwave signal ($\Delta A/A$) and the phase difference²² obtained from Eq. (1), respectively, via

$$\text{Re}\{\sigma_{xx}\} = d \cdot \frac{\ln|\Delta A/A|}{Z_0 \ell} \quad (2)$$

and

$$\text{Im}\{\sigma_{xx}\} = d \cdot \frac{\Delta \phi_s}{Z_0 \ell}. \quad (3)$$

Figure 10 shows the $\text{Re}\{\sigma_{xx}\}$ and $\text{Im}\{\sigma_{xx}\}$ of sample A at 6.99 GHz for B between 3 and 10 T. The scale bar on the plot is 10 μS for both curves. The peak power into the sample was about -85 dBm, and the equivalence average power was only about -105 dBm. The $\text{Re}\{\sigma_{xx}\}$ curve shows clear broad minima near zero conductance around integer Landau level filling factors (ν), while the $\text{Im}\{\sigma_{xx}\}$ curve exhibits a concave shape in the plateau regime and a deep minimum in the transition region between adjacent Hall states. This observation is very similar to what Hohls *et al.*⁹ reported; however, compared to their presented data (Fig. 2 in Ref. 9), our data give a much less background noise than theirs. The background fluctuation for both curves in Fig. 10 is only about 50 nS.

Sample B is fabricated from a typical MBE-grown modulation-doped GaAs/AlGaAs heterostructure containing a 2DES, which is 150 nm under the surface. The mobility of the 2DES is $1.6 \times 10^5 \text{ cm}^2/\text{Vs}$ at 4 K, and the density is $1.02 \times 10^{11} \text{ cm}^{-2}$. The 2DES under the CPW pattern was first removed by chemical etching before the metal-film deposition. The 2DES left in the gap was then patterned into about 7000 identical QW mesas, each of $0.7 \mu\text{m}$ wide and $20 \mu\text{m}$ long, by using e-beam lithography and chemical etching. Other experimental details can be found in our previous publication.¹⁰ Figure 11 shows a typical data, including both the amplitude change and the phase variation as a function of B . The peak power of the pulsed microwave signals used in this measurement was -50 dBm (about -66 dBm in average) before being fed into the sample. The amplitude and phase

FIG. 11. (Color online) Relative amplitude change (ΔA) and the phase variation ($\Delta \phi_s$) of a CPW containing a QW array in the slots.

fluctuations in ΔA and $\Delta \phi_s$ data are less than 0.003% and 0.001° , respectively. The Landau level filling factor (ν) is assigned according to the electron density in each QW from the Shubnikov–de-Haas oscillations observed in high-frequency data.¹⁰

In summary, we have developed and demonstrated a high-sensitivity vector detection system for very low-power microwave signals used in a CPW broadband sensor. This system is a very powerful tool in studying the dynamic behaviors of LDESs at low temperatures.

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- ¹⁷Maxim Integrated Products, Sunnyvale, CA.

¹⁸Intersil Corporation, Milpitas, CA.

¹⁹Analog Devices, Inc., Norwood, MA.

²⁰In this design, we need to insert a TTL inverter between the TTL1 and the control lead of the analog switch since there is a built-in inverter between input and the switch control in ADG201HS.

²¹MITEQ, Hauppauge, NY; Quinstar Technology Inc., Torrance, CA; M/A

COM, Lowell, MA; Pulsar Microwave Corp., Clifton, NJ; Agilent, Palo Alto, CA.

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