A 2-V 10.7-MHz CMOS Limiting Amplifier/RSSI

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Abstract—This paper presents low-voltage low-power CMOS circuit design techniques for an intermediate frequency (IF) limiting amplifier and received signal strength indicator (RSSI). The architecture of the limiting amplifier and RSSI employed is determined by the optimal power consumption for a specified speed, overall gain, and accuracy. Each gain cell of the limiting amplifier employs folded diode load for low-voltage operation. Offset is reduced by a cross-connected source-coupled pair offset subtractor that is along the signal path. Full-wave current rectification and summation are employed in the RSSI circuit to achieve high precision while maintaining low voltage and low power. Using a single 2-V supply voltage, measured results demonstrate the input dynamic range is larger than 75 dB for 10.7-MHz IF application. The prototype occupies an active area of 0.4 mm² using a 0.6-µm digital CMOS technology. The power dissipation is 6.2 mW.

Index Terms—CMOS analog integrated circuit, IF amplifier, radio receiver, RSSI, wireless communication.

I. INTRODUCTION

A TYPICAL wireless receiver block diagram that is widely employed in FM radio, cellular telephone, and other communication systems is shown in Fig. 1 [1]. Magnitude control is critical in wireless applications since the signal received has a wide dynamic range. One or two IF stages with the aid of bandpass filters in the heterodyne receiver can distribute the required total gain and, in addition, suppress the large out-band interference. This structure alleviates the dynamic range requirement of the analog-to-digital interface if compared with the direct-conversion method. A magnitude-control amplifier that is always at the last stage of the IF processor keeps the signal constant for further demodulated. The magnitude control can be a limiting or an automatic gain control (AGC) amplifier. A limiting amplifier composed of a chain of gain stages saturates the input signal to a constant level. A limiting amplifier rather than an AGC is widely employed in wireless IF because it can handle a larger dynamic range while consuming less power with simple circuitry.

A received signal strength indicator (RSSI) is normally employed to represent the received signal strength. It can also be used to adjust the gains of the RF front-end and baseband processors, and power down the receiver when there is no signal. The RSSI is generally realized in logarithmic form because the wide dynamic variation of the received signal can be represented within a limited indication range. Successive-detection architecture is adopted for realizing the logarithmic amplifier. It is essentially composed of several full-wave rectifiers and a low-pass filter, which are in combination with the existing limiting amplifier circuits. Thus successive-detection is power efficient.

Fig. 2 shows the architecture adopted for an IF 10.7-MHz limiting amplifier and RSSI. Voltage and current-mode circuit design techniques are incorporated to achieve low voltage and low power. In this paper, the architecture designs are described in Section II. Circuit design techniques of the proposed CMOS limiting amplifier and RSSI are presented in Section III. Section IV shows experimental results. Finally, conclusions are drawn in Section V.

II. ARCHITECTURE DESIGNS

A. Limiting Amplifier

The architecture of the limiting amplifier employed is a cascaded structure as shown in Fig. 2. The number of the limiting amplifier gain cells associated with gain, bandwidth, and power determines optimal overall circuit performance.

Assuming a limiting amplifier composed of \( N \) identical gain stages and requiring overall small signal gain \( A_L \) and bandwidth \( f_s \), then the normalized gain \( A_s \) and the bandwidth \( f_s \) of each gain stage can be derived as

\[
A_s = A_L^{(1/N) - 1}
\]

\[
f_s = \frac{1}{\sqrt{2I_N - 1}}.
\]

Fig. 3(a) shows the relationship among the gain, bandwidth, and stage number for a system that requires an overall gain \( A_L \) of 80 dB. Once the overall gain and bandwidth of the limiting amplifier are specified, the voltage gain of each stage is obviously reduced as the cascading number of stage increases. However, this introduces more poles cascaded since the number of gain stage increases. The bandwidth of each stage therefore has to be increased in order to maintain an overall bandwidth. Curve A in Fig. 3(b) depicts the normalized gain-bandwidth product \((G \cdot BW)\) of each gain stage versus the stage number. There is an optimum stage number, namely \( 2 \cdot \ln(A_L) \), which requires the minimum \( G \cdot BW \) of each stage [2].

Power minimization in the IF stage of wireless application is more a practical issue. The total power consumption of a limiting amplifier is a product of the stage number and the power dissipation at each stage. Once the stage number increases, the total power increases linearly; on the other hand, the \( G \cdot BW \) requirement for each stage, as depicted in curve A of Fig. 3(b), is alleviated. In the following, the relationship between \( G \cdot BW \) and the power of a single gain stage will be shown. The optimal number of stages for minimal power dissipation can therefore be determined.

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Assuming each identical gain cell is a one-pole system, the $G \cdot BW$ of each stage can be expressed as

$$G \cdot BW = \frac{g_m}{C} = \frac{\mu C_\text{ox}(W/L)(V_{GS} - V_t)}{k \cdot W L} \propto \frac{V_{GS} - V_t}{I^2}$$  \hspace{1cm} (3)$$

$$= \frac{\sqrt{2} \mu C_\text{ox}(W/L)I_d}{k \cdot W L} \propto \sqrt{\frac{I_d}{WL^3}} = \sqrt{\frac{P}{V_{DD}Wl^3}}$$  \hspace{1cm} (4)$$

where $k$ is a scaling factor, $I_d$ is the bias current of the amplifier, $V_{DD}$ is the supply voltage, and $P$ is the power consumption. Other notations in (3) and (4) are common in the usual sense of MOS device parameters. Equation (3) shows that if the device channel length is fixed, the gain-bandwidth product is dictated by the gate overdrive voltage $V_{GS} - V_t$. Prudent use of $G \cdot BW$, while keeping device size unchanged, will reduce the power for a given device in a quadratic manner as indicated in (4).

The power $P_t$ of the overall amplifier is shown in curve B in Fig. 3(b). It is proportional to the number of stages $N$ and can be described as

$$P_t = N \cdot P_s \propto N \cdot (G \cdot BW)^2$$  \hspace{1cm} (5)$$

where $P_s$ is the power of each stage. There exists another trade-off between the stage number and $G \cdot BW$ for power optimization. For an 80-dB dynamic range, seven stages are chosen based on minimum power dissipation and required $G \cdot BW$.

Besides power optimization, there is another practical issue, which is AM-to-PM conversion. It is particularly a problem in high-speed limiting-amplifier applications. This output phase modulation caused by input amplitude variation is mainly due to different delays of bandwidth-limited gain cell for different input levels. This phase variation will degrade the receiver demodulation performance. The phase variation can be expressed in term of input signal band $f_{in}$ and gain cell bandwidth $BW$ as

$$\Delta \phi = 17.6 \cdot \left( \frac{f_{in}}{BW} \right) \cdot N.$$  \hspace{1cm} (6)$$

The bandwidth of each gain cell therefore has to be properly determined for a specified phase variation.

**B. Received Signal Strength Indicator**

A logarithmic amplifier is widely used in the RSSI, since a wide dynamic variation of signal power can be represented within a limited voltage range. Successive detection, as shown in Fig. 2, is based on piecewise-linear approximation [4]. Each section is obtained by rectifying each gain cell output of the limiting amplifier. The precision of the RSSI is mainly determined by the number of sections, i.e., the stage number of the...
Fig. 3. Performance versus the number of gain stage when total gain is 80 dB. (a) Gain and bandwidth. (b) Speed and power. For ease of comparison, all parameter values are normalized to the case of a single gain stage and expressed in logarithm.

Fig. 4. Evaluation of RSSI maximum error versus number of stage.

III. CIRCUIT DESIGNS

A. Limiting Amplifier

Simple circuitry is the norm for high-frequency low-power circuit designs [5]. Some techniques are proposed to overcome circuit constraints associated with the low-voltage operation. A gain stage of the limiting amplifier can be a conventional simple source-coupled pair with diode load as shown in Fig. 5(a). However, this circuit configuration can hardly work at 2 V using standard CMOS technology because the n-type MOS transistors (M1, M2) inherently possess body effect. In addition, since the input and the output have to be biased at the same dc level for direct cascading, the minimal supply voltage required is \( V_{DD} \), where \( V_{DD} \) is the turn-on voltage of the corresponding device M1, \( V_{DD} \) is the overdrive voltage of the MOS transistor, and \( V_{swing} \) is the signal swing.

Fig. 5(b) shows the proposed gain cell circuit. The diode connected transistors \( M_3 \) and \( M_4 \) are folded to ground as loads that parallel to the input source-coupled pair transistors \( M_1 \) and \( M_2 \). It is a folded-circuit technique to reduce the supply voltage. The voltage gain of this circuit can be shown as

\[
A_v = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{W}{L}} \frac{I_{D1}}{I_{D3}}.
\]

The voltage gain of the folded load is determined by the bias current and the device ratios. Both ratios can be designed to be insensitive to process and thermal variations. This folded diode load involves a little circuit overhead. However, the minimum
supply voltage can be reduced to $V_{DD} + 3\Delta V + V_{swing}$. The supply voltage therefore can be 2 V or lower. Though the folded loads consume some extra current, it is insignificant if compared with the advantage of a lower supply voltage.

Offset cancellation is essential in limiting amplifier design, since any offset caused by device mismatch may be so large that it smears the small input signal. A feedback-type offset cancellation mechanism, as shown in Fig. 2, rather than a feedforward structure is employed in this design, because it introduces less circuits overhead [6]. The input offset voltage of this negative feedback cancellation is reduced by a factor of the cascaded voltage gain of the forward path [7].

The employed offset cancellation dc feedback circuit is shown in Fig. 2. An n-well resistor and an external capacitor filter the high-speed data waveform of the limiting amplifier output, and extract the dc offset voltage. An offset subtractor then subtracts the feedback dc offset information ($V_{o1} + V_{o2}$) from the input IF signal ($V_{in1} + V_{in2}$) as shown in Fig. 6. The subtracting operation is accomplished by the cross-connected circuit topology. The subtractor circuit that is along the signal path introduces insignificant amount of parasitics, which will not degrade the overall speed. The voltage gain of the voltage subtractor is 0 dB.

B. RSSI

The RSSI shown in Fig. 2 is an architecture of piecewise-linear approximation. Each piece of linear section is obtained by rectifying each gain cell output of the limiting amplifier first. All the rectified waveforms are then summed and filtered to yield a dc-like indicating voltage. Cascaded gain cells are already existent in limiting amplifier, therefore only full-wave rectifiers (FWRs) and a lowpass filter that ties all the FWR outputs are required in addition to the RSSI.

There are several published circuit approaches [8], [9] available for rectification. However, they either consume too much power or are not suitable for low-voltage 2-V operation. An open-loop current-mode rectification structure as shown in Fig. 7(a) is developed for low-voltage and low-power requirements. The conceptual circuit diagram is shown in Fig. 7(b). When the input current $I_{in}$ flows into or out from the rectifier, it switches devices $M_{PD}$ and $M_{PN}$ ON and OFF respectively. A half-wave rectified current $I_{rec}$ is therefore established at output. A full-wave rectification, on the other hand, can be obtained by utilizing two identical paths in parallel, which are driven by a pair of differential input currents. Two additional circuit techniques, namely, nMOS substitute and pre-bias...
techniques, are employed in order to obtain a better precision during fast switching. The former replaces the pMOS device \( M_{DP} \) of current sink to ground with an nMOS diode. This alternation improves the speed performance due to less parasitics of the nMOS device [10]. The other technique used is the pre-bias method. The voltage \( V_{bi} \) biases two switches at the nearly-on condition. Consequently, only a small amount of change of input current makes the switch fully ON or OFF. This reduces the error caused by extra current when one switch is ON while the other is not completely OFF, which can be significant for high-speed under low-voltage operation.

Devices \( M_{D1} \) to \( M_{D4} \) of the complete full-wave current rectifier, as shown in Fig. 7(a), form transconductance stages that convert the differential input voltages to currents. The transistors \( M_{T1} \) to \( M_{T4} \) following serve as the current mode FWR. Transistor pairs \( M_{T1} \) and \( M_{T2} \), \( M_{T3} \) and \( M_{T4} \) are turned on alternatively in each half period. A full-wave rectified current \( I_{OUT} \) is thus obtained at the output. This structure possesses high precision while dissipating low dc current. Most important of all, the minimum supply voltage for a functionable circuit is \( V_{rs} + 2\Delta V + V_{sweep} \), which is therefore suitable for 2-V operation or less.

The rectified current at output of each FWR is summed and filtered to a first-order passive low-pass filter. The associated resistor and capacitor are external, thus the RSSI output slope and filter bandwidth are adjustable.

IV. EXPERIMENTAL RESULTS

Fig. 8 is the die photo of the proposed 10.7-MHz limiting amplifier and RSSI. It is implemented in a standard 0.6-\( \mu \)m CMOS digital technology. The active area is 0.4 mm\(^2\). Power consumption is 6.2 mW using a 2-V single supply voltage. Fig. 9 shows frequency responses of the limiting amplifier first three stages. Each stage provides a voltage gain of 12 dB with a bandwidth of 70 MHz, which is seven times larger than
the signal band in order to decrease the AM-to-PM effect. Measurement results demonstrate that the phase variation is less than 5° for an input dynamic range more than 60 dB. The limiting amplifier -3 dB input sensitivity, which is defined as the input power that causes output power 3 dB lower than the saturated constant level, is -78 dBm, as shown in Fig. 10. The input referred noise is 10 μVrms. The input equivalent offset voltage is less than 2 μV with the aid of offset cancellation mechanism.

The RSSI performance is shown in Fig. 11. An external resistor of 8.3 kΩ and a capacitor of 1 nF are used to convert the summed RSSI current to voltage and simultaneously extract the dc value. The nominal slope of the indication curve measured is 10.8 mV/dB@83KΩ load. The indication range is wider than 75 dB within ±1 dB linearity error.

Table I lists the performances of the proposed limiting amplifier and RSSI.

| Measured Performances of the Proposed 10.7-MHz CMOS Limiter Amplifier/RSSI |
|---------------------------------|-----------------|
| Technology                      | 0.6μm SPTM Digital CMOS |
| Limiting Amplifier              | 12 dB            |
| Single stage gain               | 70 MHz           |
| Input referred noise            | 10μVrms          |
| 3dB Sensitivity                 | -78 dBm          |
| Input equivalent offset voltage | < 2 μV           |
| RSSI                            | 75dB             |
| Nominal slope                   | 10.8mV/dB@83KΩ  |
| Logarithmic linearity error     | < ± 1 dB         |
| Supply Voltage                  | 2-V              |
| Power Consumption               | 3.1 mA           |

V. Conclusion

Low-voltage low-power CMOS circuit design techniques for 10.7-MHz limiting amplifier and RSSI applications were presented in this paper. A seven-stage amplifier architecture was derived under minimum power consideration. Each gain cell employs folded diode load structure rather than the conventional diode load for supply voltage of 2 V or less. The dc offset voltage is cancelled by an offset subtractor which composed by a cross-connected source-coupled pair. Current mode FWRs that construct the RSSI successive detection adopt a pre-bias technique and use all nMOS devices along the signal path to enhance speed. Sensitivity of -78 dBm and an indication range of 75 dB within ±1-dB linearity error were measured. The prototype is implemented in 0.6-μm digital CMOS technology and occupies an active area of 0.4 mm². It consumes 6.2 mW from a 2-V power supply.

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References


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