HD3 = -67.1 dB. In the proposed cell, the second harmonic is at the noise level, approximately -114 dB, while the third harmonic is negligible (<-130 dB). In both cases, a sinusoidal input signal of frequency 5 kHz and modulation index $M_I = 0.5$ was used, with a sampling rate of 512 kHz.

One additional advantage of this cell is the suitability for low-voltage operation. Simulations have been carried out for supply voltages as low as 1.8 V, without any boosting circuitry for the clock signals. This is achieved with a marginal degradation of the distortion behavior. This performance is possible because the drain and source nodes of the switches are always kept at a voltage near the rail, allowing enough overdrive for settling purposes. This is difficult to achieve in SC circuits, even if the most recent techniques proposed by Baschirotto *et al.* [11], Fujimori *et al.* [12], and Steyaert *et al.* [13] are used.

In practice, the major limitations of the proposed cell are the mismatches between the charge redistribution factors and between the memory capacitors. Fig. 4 shows the effect of these two types of mismatches in the cell. They indicate that a second harmonic of about -90 to -100 dB can be achieved, with minimum-size switches and a careful layout.

IV. CONCLUSION

We propose a very low-distortion fully differential switched-current memory cell. SPICE simulations with a behavioral model for the charge injection show harmonic distortion levels of about -90 to -100 dB, which are two orders of magnitude below the harmonic distortion in basic cells. We have analyzed the effects of mismatches on critical components, and conclude that with careful design and layout, a very low harmonic distortion level is to be expected.

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A 155-MHz BiCMOS Automatic Gain Control Amplifier

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Abstract—This paper proposes a 155-MHz automatic gain control (AGC) amplifier implemented in a double-poly-double-metal 1.0- μ m BiCMOS technology. The amplifier contains an exponential-type variable-gain amplifier, a buffer-based filter, and asynchronous demodulation peak detector circuits. The initialization and the output magnitude setup circuits are incorporated in the AGC amplifier. It yields an input dynamic range of at least 26 dB and provides a constant output of 1 V_{pp} at a 50- Ω load with AGC loop bandwidth of 80 kHz. The power consumption is 180 mW from a single 5-V supply.

Index Terms—Amplifier, analog integrated circuits, BiCMOS integrated circuits.

I. INTRODUCTION

In a data-transmission system such as Synchronous Optical Network (SONET), the transmitted signal through different amounts of attenuation channel results in a wide range of signal levels at the receiving end. Control of a constant output-signal magnitude for the succeeding timing-recovery and data-regeneration circuits is required. A block diagram of a typical optical receiver is shown in Fig. 1. The automatic gain control (AGC) amplifier and limiting amplifier are the two postamplifier techniques for maintaining a constant output signal amplitude against the received optical power variation. In this paper, an AGC amplifier with a closed-loop format is chosen because it is less sensitive to environmental and process variations. Furthermore, this type of amplifier can remove the low-frequency noise [1].

The designed AGC is for short-haul (15 km) SONET OC-3 application with an input dynamic range of 26 dB (20-400 mV_{pp}) and a bit rate of nonreturn-to-zero (NRZ) 155.52 Mb/s. Thus, as examples, the high-speed circuits, variable-gain amplifier, low-pass filter (LPF), and peak detector are all very crucial. The LPF is a fourth-order Bessel type that requires a -3-dB cutoff frequency of 116 MHz. It employs the proposed cascaded fully differential Sallen and Key biquad structure using a cascode unity-gain buffer. Asynchronous

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Fig. 1. Block diagram of a typical optical receiver.

Fig. 2. Proposed architecture for the BiCMOS SONET OC-3 AGC.

demodulation is used in the peak detection for fast system response. An initialization that sets up the variable gain amplifier (VGA) gain in the middle imbalances the AGC loop, besides nulling the loop offset, to ensure a proper biasing condition for a negative feedback mechanism when the loop is initially closed.

The circuit is implemented in a double-poly-double-metal 1.0- μm BiCMOS technology with a single 5-V power supply. The advantages of bipolar junction transistors (BJT's) and MOS transistors are exploited in this automatic gain-control amplifier circuit [1]–[3]. High-speed and large driving capability analog functions can be achieved by using BJT transistors.

The rest of the paper is organized as follows. Architecture with AGC output magnitude setup and loop initialization will be described in Section II. The corresponding circuit designs of the forward and feedback paths will be presented in Section III. Experimental results will be given in Section IV and finally, the conclusions in Section V.

II. ARCHITECTURE

The architecture of the proposed 155-MHz AGC amplifier is shown in Fig. 2. It is composed of a forward path and a feedback path. In the forward path, the VGA is controlled by a feedback-path dc-like signal V_{gc} . The following linear-type amplifier (Amp1) provides a 12-dB gain. The very high-frequency LPF with its -3 -dB bandwidth at 116 MHz is a fourth-order Bessel–Thompson filter that is used to minimize the intersymbol interference. A subsequent linear-type amplifier (Amp2) provides an additional 8-dB gain. The 6-dB slicer/driver of the last stage drives the following functions, namely timing recovery and data regeneration (Fig. 1).

The AGC feedback path circuits as shown in Fig. 3 include a peak detector, an AGC output magnitude setup circuit, an initiator, and an integrator. The peak detector with a one-pole filter features a self-generated clock to extract the amplitude information, which will be integrated to a dc-like VGA control signal V_{gc} . The integrator that acts as a comparator integrates the feedback signal around a reference voltage to obtain the voltage V_p . The gain stage amplifies the voltage

V_p to yield the VGA control voltage V_{gc} . When the whole AGC loop is constructed, the speed/phase of every block must be carefully designed in order to ensure a negative feedback loop. Furthermore, the dc current $I_{initial}$ offsets the loop in the proper bias once the loop is closed. A tuning voltage V_{set} is introduced to set up the output swing magnitude and also to overcome the integrated circuit (IC) process variation. Fully differential circuit architecture is employed in the linear channel for larger swing and better power-supply-rejection ratio (PSSR).

Following the analysis given by Wang etc. [4], AGC loop parameters, namely, poles of the feedback path low-pass filter, unity-gain frequency of the integrator, and hence the AGC loop bandwidth, can be calculated for analysis. The design values of the initialization dc-current $I_{initial}$, the output magnitude-control current I_{set} in the feedback path can also be calculated using the proposed approach provided by [4]. More precise values that provide loop circuit design specification were derived practically from a complete AGC closed-loop simulation in C program.

III. CIRCUIT DESIGNS

In this section, circuit designs of the key function blocks, namely VGA, low-pass filter, peak detector, loop initialization, and output magnitude set-point will be presented.

A. VGA

The VGA circuit as shown in Fig. 4 is composed of a Gilbert cell-type amplifier (transistors Q_1 – Q_6) and an emitter follower (transistors Q_7 – Q_8). This VGA amplifier is designed with curve-fitted exponential gain characteristics, controlled by the feedback signal V_{gc} , in order to maintain a more stable AGC loop bandwidth than that provided by a linear type [4].

This nonlinear gain relation is obtained by choosing a proper resistor value (R_{E1} – R_{E4}) of the Gilbert cell (transistors Q_1 – Q_6) shown in Fig. 4 with a control voltage V_{gc} and tail current I_{C5} . Resistor values of R_{L1} , R_{E1} , and R_{E5} , on the other hand, are chosen in conjunction with the bias current for the desired output swing v_{out} , the nonlinear start-up control voltage V_{gc} , and the designed input-swing V_{in} , respectively. In the design, when the feedback signal V_{gc} changes from 50 to 360 mV, the VGA amplifier retains a curve fitted exponential characteristics of gain relation from -18 to 8 dB. The minimum -3 -dB bandwidth of the exponential type VGA required is at least 116 MHz [5].

B. Low-Pass Filter

The low-pass filter after the Amp1 is a waveform-shaping filter (Fig. 2). It is a fourth-order Bessel–Thompson filter with -3 -dB bandwidth at 116-MHz, as shown in Fig. 5(a). This filter is a cascaded biquad filter. Unlike the conventional op-amp-based active filter, each biquad used in this design is a fully differential buffer-based architecture that uses a BJT cascode unity-gain follower [shown in Fig. 5(b)]. Here, the cascode transistors (Q_{11} – Q_{14}) are used to reduce the Miller effect. Therefore, the buffer-based filter has a much wider bandwidth and higher speed than the conventional operational amplifier-based filter. Unity gain is provided by the resistor unity ratio of the load R_{L11} to the degenerated resistor R_{E13} . Values of the resistors R_{L11} and R_{E13} chosen, on the other hand, are in conjunction with the maximum output and the maximum input swings, respectively. Emitter followers are used in the front (Q_9 – Q_{10}) and the rear (Q_{15} – Q_{18}) for buffering. The -3 -dB bandwidth of the unity-gain buffer is better than 1 GHz.

All the resistors in this fully differential biquad-cascaded Sallen and Key filter are chosen of the same type. Though filter -3 dB

Fig. 5. (a) A cascaded biquad fourth-order Bessel-Thompson shaping filter. (b) The fully differential unity-gain follower.

Fig. 6. Proposed rectifier-type peak detector with a one-pole low-pass filter.

Fig. 7. The die photo of the SONET OC-3 receiver chip. The top portion is the AGC of this paper.

Fig. 8. The AGC output eye patterns with input magnitudes 20 mV_{pp}, 80 mV_{pp}, 200 mV_{pp}, and 400 mV_{pp} at NRZ 155.52 Mb/s.

circuits of the proposed balanced buffer-based cascaded BJT biquad filter of -3-dB frequency 116 MHz, the negative feedback loop initialization, and the output magnitude setup. It meets the SONET OC-3 performance requirement for a short-haul application.

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Design and Analysis of High Performance Current Reference Generators for Low-Power CMOS Data Converters

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Abstract—Based on a highly accurate current divider using switched-current technique without the need of well-matched components, a current reference generator (CRG) circuit is developed to generate and hold the weighed currents used in the data converters. This paper also presents a methodology for designing high-performance CMOS CRG circuits for low-power applications and their performance analysis for estimating the accuracy, speed, and power consumption. To demonstrate the design procedure and performance analysis, several design examples are given. The simulation results show that, for a 6-bit CRG circuit, its calibration time and holding time are 27 and 242 μs , respectively, and for a 8-bit CRG circuit, they are 48 and 236 μs , respectively. The circuit consumes 1.8 mW and achieves better than 10-bit accuracy, where a MOSIS SCNA20 $2\text{-}\mu\text{m}$ process and a 3.3-V supply voltage are employed. Thus, the developed CRG circuit is well suited for low-power/low-voltage and moderate resolution data converters.

I. INTRODUCTION

A class of analog circuits wherein current rather than voltage is the primary signal medium has been received considerable attention recently [1]–[6]. The switched-current (SI) technique couples itself well with the down-scaled CMOS technology and creates a potential for speed improvement. Since highly linear capacitance is not needed for high-accuracy analog signal-processing circuits with SI technique, the same low-cost digital CMOS process for the digital portion of

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