A Systematic Design to Suppress Wideband Ground Bounce Noise in High-Speed Circuits by Electromagnetic-Bandgap-Enhanced Split Powers

Chien-Lin Wang, Guang-Hwa Shiue, Wei-Da Guo, and Ruey-Beei Wu, *Senior Member, IEEE*

Abstract—In this paper, the split power planes with electromagnetic bandgap structures enhancement is proposed for the wideband suppression of ground bounce noise in high-speed printed circuit boards. A systematic design procedure is presented, featuring a modified analytic design formula, a novel compact electromagnetic bandgap layout, and a discussion on the minimum number of cascaded rows. As it is capable of selectively suppressing the ground bounce noise at several desired frequencies, the approach is applied to deal with the coupled noise between two isolation islands and the ground bounce noise induced by signal line crossing the split power planes. Successful noise suppression over an ultrawide band from dc to 5 GHz and reduction of the peak ground bounce noise in the time domain by 75% by an electromagnetic bandgap strip 1.44 cm wide is demonstrated. Good agreement is seen from the comparison between simulation and experimental results.

Index Terms—Electromagnetic bandgap (EBG), electromagnetic (EM) interference, power integrity, signal integrity, simultaneously switching noises, split power plane.

I. INTRODUCTION

GROUND bounce noise, also known as simultaneous switching noise, is becoming one of the major concerns in high-speed digital circuits with faster data rates and lower voltage levels. This noise can produce false switching in digital circuits and breakdown in analog circuits. Mainly due to the high-speed time-varying currents through vias in the parallel-plate layer, it may cause significant signal integrity problems and electromagnetic (EM) interference in high-speed circuits [1], [2]. With the increasing clock frequencies of digital circuits, the ultra-wideband noise suppression from dc to several gigahertz becomes a critical design consideration.

Several different methods for ground bounce noise reduction have been proposed in the literature. Adding decoupling capacitors [3] is the most commonly used approach, as they can provide grounding paths for the voltage fluctuations on the reference dc voltage planes, but the performance at high frequencies

is limited by the increasing impedance of equivalent series inductance. Dividing the power plane into power islands can also help isolate the noisy elements. However, its resonance at certain frequencies will cause significant coupling noise [4]. It is also reported that significant ground bounce may occur due to the signal lines crossing split power planes [5], which is another mechanism magnetically dual to the via-induced ground bounce. To achieve better performance, one may employ embedded capacitors [6] through the use of an additional layer of high dielectric material. One may also introduce the cascaded electromagnetic bandgap (EBG) structures [7] to the ground plane, which occupy large areas for suppressing all resonant frequencies and is deficient in reducing wideband noise. All of these methods suffer from either limited bandwidth in noise reduction or expensive manufacturing process.

Recently, a new idea of using EBG structures embedded periodically between the parallel plates has been proposed and can provide good suppression of ground bounce noises at frequencies over several gigahertz [8], [9]. A simple circuit model for one unit cell of an EBG structure is even proposed with equivalent L and C at a given resonant frequency [10]. However, time-consuming full-wave analysis is usually required to calculate the S -parameter and dispersion diagram for the design of EBG structures.

Given the noise suppression by split planes for low frequencies, it is interesting to investigate the enhancement at high frequencies due to the employment of EBG structures. The primitive simulation results showed that EBG combined with a split plane is able to provide wideband ground bounce suppression [11]. In this paper, we have elaborated on the idea and a systematic analysis and design procedure is presented for an efficient method of designing EBG structures with more accurate design formula, a novel EBG layout for the size reduction, and the required numbers of rows for sufficient noise suppression. The proposed procedure is then applied to suppress ultra-wideband coupled noise between isolation islands and slot-induced ground bounce by signal lines crossing split power/ground planes, while maintaining the signal transmission quality within the required specifications for common signaling standard.

The organization of this paper is as follows. After a brief statement of the problem, Section II describes the systematic procedure for the design of compact EBG structures. Some numerical examples to demonstrate its performance in noise suppression are given in Section III, with experimental validation given in Section IV. Finally, brief conclusions are drawn in Section V.

Manuscript received May 3, 2006; revised August 3, 2006. This work was supported in part by the National Science Council, Taiwan, R.O.C., under Grant NSC93-2213-E-002-016 and by Inventec Incorporated.

The authors are with the Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei 106, Taiwan, R.O.C. (e-mail: r93942010@ntu.edu.tw; d90942002@ntu.edu.tw; f92942062@ntu.edu.tw; rbwu@ew.ee.ntu.edu.tw).

Color versions of Figs. 1–14 are available at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TMTT.2006.886387

Fig. 1. Noise-reduction mechanism by EBG structures within parallel plates of the power distribution network.

Fig. 3. Top view of a unit-cell EBG with: (a) rectangular layout ($N = 0$), (b) spiral layout ($N = 1$), and (c) spiral layout ($N = 2$). (d) Side view of a unit-cell EBG embedded within parallel plates.

(a)

(b)

(c)

Fig. 2. (a) Top view of split power plates. (b) Side view of two isolation islands with via-induced ground bounce. (c) Side view of signal-line-crossing split power plates with slot-induced ground bounce.

II. COMPACT EBG DESIGN

A. Statement of the Problem

Consider split power planes in a printed circuit board with the enhancement of noise suppression by EBG structures. Fig. 1 demonstrates the noise generation and radiation as well as the suppression mechanism by means of the split planes and EBG structures.

The split planes are commonly used in high-speed digital circuits for isolation of noisy elements and/or provision of multiple power sources. Since power planes are separated by slots as in Fig. 2(a), the noise from different power islands can be isolated at least for lower frequencies. However, there is still significant

noise coupling between two isolation islands at resonant frequencies [4]. For example, for rectangular planes with size $a \times b$, the resonant frequencies are given by

$$f_{mn} = \frac{1}{2\sqrt{\mu\epsilon}} \sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2}. \quad (1)$$

In addition, there are two main ground bounce noise-generating mechanisms within the split parallel plates, either by fast switching current through vertical vias, as in Fig. 2(b), or by signal propagating across the slot [5], as in Fig. 2(c). The noise propagates between the parallel plates and may deteriorate the noise isolation by the split planes at aforementioned resonant frequencies. The EBG structures with band rejection effects can help reduce the noise coupling. It is desired to have a systematic design procedure for the EBG structures which may exhibit sufficient noise suppression, but occupy only a small area.

B. Design of Center Band-Reject Frequency

Within split power planes, ground bounce noises usually propagate at specific frequencies as in (1). For achieving wide-band noise suppression, EBG with several rejection frequency bands is important for the suppression mechanism shown in Fig. 1.

The unit-cell EBG structure is shown in Fig. 3, which includes a layer with metallization layout and shorted with the ground through a center via connection. In contrast to the traditional square patch layout [10], a novel spiral type is proposed here for the size reduction. The layouts with number of turns $N = 0, 1, 2$, are shown in Fig. 3(a)–(c), respectively. Other important parameters for the unit-cell spiral EBG are the gap s and width w of the spiral line.

Note that the special case with $N = 0$ corresponds to the traditional EBG of a rectangular patch layout [8], [9] and equivalent model [10]. In order to predict the center frequency of the spiral EBG rejection band, a revised equivalent circuit model is shown in Fig. 4(a), in which the circuit elements are given by

$$C_1 = C_2 = \epsilon_r \epsilon_0 \frac{d^2}{h_v} \quad (2)$$

$$L_v = \mu_0 \frac{h_v}{2\pi} \left[\ln \frac{2h_v}{r_v} + \alpha \right] \quad (3)$$

Fig. 4. (a) Equivalent circuit of a unit cell of an EBG. (b) Inductance formula derived from the image theorem.

and, hence, the center band-reject frequency

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{(L_v + L_s)(C_1 + C_2)}}. \quad (4)$$

In this model, C_1 and C_2 denote the capacitance between the EBG structure and the top and bottom plates, respectively, and L_v and L_s denote the inductance of the via and spiral EBG layout. For the via inductance (L_v), it is worth mentioning that the inductance formula is suitable only for the cases in which via radius r_v is much smaller than layer height h_v , and the constant α is determined empirically from the full-wave simulation results [10].

A general form of the inductance formula can be revisited if the image theory is applied to substitute the lower ground plane as in Fig. 4(b). As a result, the inductance equals one half of that of a single via of total length $2h_v$, for which the exact formula is available. From the internal and external inductances for a round via, the inductance formula can thus be given by

$$\begin{aligned} L_v &= \frac{1}{2} L'_v(2h_v) \\ &= \mu_0 \frac{h_v}{2\pi} \left[\ln \left(\frac{2h_v}{r_v} + \sqrt{1 + \left(\frac{2h_v}{r_v} \right)^2} \right) \right. \\ &\quad \left. - \sqrt{1 + \left(\frac{r_v}{2h_v} \right)^2} + \frac{r_v}{2h_v} + \frac{1}{4} \right]. \end{aligned} \quad (5)$$

Fig. 5. Comparison of the simulated results of via inductance versus h_v/r_v with those of the analytic design formula.

In case of long vias ($r_v \ll h_v$), it is worth noting that (5) can be reduced to (3) with $\alpha = -0.056$.

In order to verify the accuracy of the inductance formula, the full-wave simulation results below the resonant frequency are compared with those by traditional formula (3) with $\alpha = -0.1$ and the present modified formula (5). In Fig. 5, with the increase of h_v/r_v , it can be seen that (3) deviates significantly from the full-wave simulation result [14], while (5) can yield accurate results as h_v/r_v varies from 0.5 to 4. Note that the inductance is important in accurately determining the band-reject frequency of the EBG structures as given by (4).

It is evident from Fig. 1 that significant board area will be occupied by the EBG structures, which limits the available real estate for circuit layout. The spiral EBG layout ($N \neq 0$), having larger equivalent inductance ($L_v + L_s$) than the rectangular patch design, can provide the advantage of size reduction. However, the inductance of spiral structures is difficult to derive, and one should resort to numerical simulation. By choosing different s , w , and N , the inductance of the spiral EBG inductor can be derived from numerical model extraction as well. The extracted spiral layout inductances (L_s) are shown in Fig. 6. It is considered that the advantage of introducing a spiral inductor is to add one more variable for controlling the center band frequency of EBG rejection, in addition to the size of square patch d to control C_1 and C_2 .

For the analysis of spiral EBG structures, a dispersion diagram is usually used to derive the bandstop region. In the simulation setup for dispersion relation extraction, a unit cell (e.g., spiral patch, power plate, ground plate, via, or dielectric materials) is considered. The full-wave simulator [14] is employed to calculate the resonant frequencies versus the two-dimensional (2-D) propagation vectors. The frequency band over which there are no propagation modes depicts the bandgap region of the EBG structures.

Fig. 7 compares the dispersion diagram between a rectangular ($N = 0$) EBG with width $d = 9.5$ mm and a spiral EBG with $N = 1$ and width $d = 4.9$ mm ($w = 1.5$ mm and $s = 0.2$ mm). The via height is fixed at $h_v = 0.77$ mm and substrate height at

Fig. 6. Equivalent inductance of spiral EBG layout ($h_v = 0.77$ mm).

Fig. 7. Dispersion diagram for spiral EBG structure ($N = 1$, $w = 1.5$ mm, $s = 0.2$ mm, and $h_v = 0.77$ mm) and rectangular EBG ($d = 9.5$ mm and $h_v = 0.77$ mm).

$t = 1.54$ mm. The center frequency of both structures is designed at 3.05 GHz with rectangular and spiral EBG design. About 75% size reduction can be achieved by spiral EBG design, but at the same time with 27% decrease in bandwidth as tradeoff. This is mainly due to the impedance mismatch between parallel-plate and EBG structures and can be compensated for with the increase of dielectric constant [12], [13].

By choosing different s , w , and N , the characteristics of spiral EBG structures are analyzed as well. The extracted center band-reject frequency and relative bandwidth are shown in Fig. 8. From these charts, given the frequency band of major noise to be suppressed, the design dimensions of the spiral EBG can be easily determined. It is also worth noting that the greater the number of turns, the greater the shrinkage on the relative bandwidth of the spiral EBG structures.

Taking one example as $f_c = 2.5$ GHz and $s = 0.2$ as constant, patch widths of 6.1 and 4 mm can be respectively derived for $N = 1$ and 2. Compared with rectangular ($N = 0$) design, patch width of 13 mm is needed for suppressing resonance at

Fig. 8. (a) Resonant frequency and (b) relative bandwidth of spiral EBG structures with slot width s as a parameter ($h_v = 0.77$ mm).

2.5 GHz. This amounts to a size reduction of 54% and 70%, respectively.

To have a compact EBG design, it is important to determine the minimum number of EBG rows that can efficiently suppress the ground bounce noise. As demonstrated in the previous work [11], employing only two rows of EBG patches are sufficient to achieve a band-reject effect of 20 dB, while more rows allow deeper band rejection. The investigations have been repeated both for the spiral EBG with $N = 1$ and 2. Although not shown here, the dependence of the band-reject characteristics on the number of EBG rows is found to be similar to that of a rectangular EBG.

III. DESIGN EXAMPLES AND NUMERICAL RESULTS

Given the design guideline for the compact EBG structures in Section II, a systematic design procedure will be discussed in this section to suppress the ground bounce noise within the split power planes. Two different kinds of ground bounce mechanisms will be considered. One is with the coupled ground bounce near the resonant frequencies of the split plates. The

TABLE I
VARIOUS EBG STRUCTURE DESIGNS FOR 2.3 AND 4.6 GHz DERIVED BY FULL-WAVE SIMULATOR [14]
(THICKNESS = 1.54 mm, $\epsilon_r = 4.4$, AND GAPWIDTH = 0.4 mm)

Entry	Patch shape	f_{center}	Patch size (mm)	(%) size reduction	Via diameter (mm)	Via height (mm)	FBW
1	Square	2.3 GHz	12 x 12	-	0.8	0.77	58.8%
2	Square	4.6 GHz	8 x 8	-	0.8	0.77	51.7%
3	N=1 Spiral	2.3 GHz	7.2 x 7.2	40%	0.8	0.77	38.5%
4	N=1 Spiral	4.6 GHz	3.7 x 3.7	54%	0.8	0.77	42.0%
5	N=2 Spiral	2.3 GHz	3.6 x 3.6	70%	0.8	0.77	31.6%
6	N=2 Spiral	4.6 GHz	-	-	0.8	0.77	-

*In entry 6, because the width of spiral line is smaller than the via diameter, it can't be realized.

other is with the slot-induced ground bounce due to signal propagating across the slot. The geometrical parameters of the spiral EBG structures with different N and their arrangement within the parallel plates will be designed.

A. Wideband Noise Suppression for Split Power Planes

Via-induced ground bounce noise happens commonly within split planes as shown in Fig. 2(a) and (b). At certain frequencies, the noise will be strongly coupled to port 2 and exhibit some power integrity concern. A remedy to enhance the noise suppression at these resonant frequencies is to employ the systematic EBG design in Section II. For example, consider the structure given in Fig. 2(a) and (b) with dimensions $a = 30$ mm and $b = 50$ mm, feeding port at the left boundary, substrate thickness $t = 1.54$ mm, dielectric constant of 4.4, and gap-width $g = 1$ mm. The first two main resonant frequencies at which the coupling noise is significant are $f_{\text{TM}10} = 2.3$ GHz and $f_{\text{TM}20} = 4.6$ GHz by (1).

The spiral EBG can be employed to reject the coupling signals at these two main resonant frequencies and achieve good ground bounce suppression over dc to 5 GHz. By using (2), (4), (5), and the design chart in Fig. 8, the geometric dimensions of the spiral EBG for different N 's are listed in Table I. For simultaneously suppressing the noise at both frequencies, two EBG structures each operating at a certain frequency are cascaded while each EBG structure consists of two rows to achieve at least 20-dB enhancement. The top view is shown in the inset of Fig. 9(a).

Assume that the rectangular EBG structures ($N = 0$) at entries 1 and 2 and the spiral EBG structures ($N = 1, 2$) as shown in Fig. 3(b) and (c) at entries 4 and 5 in Table I are realized. The noise suppression characteristics can be validated and compared by full-wave simulation [14]. Fig. 9(a) shows the coupling coefficient S_{21} versus frequency between the two isolation islands. The dotted line denotes the simulated result without EBG structures. Significant coupling noise happens near the two resonant frequencies below 5 GHz. They can be suppressed by the embedded EBG structures and achieve wideband noise reduction, as is evident from the solid curve. More than 20-dB noise suppression with rectangular and spiral EBG design is seen from dc to 5 GHz between ports 1 and 2.

Fig. 9(b) shows the time-domain results by three-dimensional (3-D) finite integration simulator [15]. In this case, a Gaussian impulse voltage source with amplitude 0.25 V and rising time of 100 ps is used as the signal excitation on port 1. Based on the present design, it can be seen that the peak coupling noise is

Fig. 9. Reduction of coupling noise by rectangular EBG and spiral EBG between isolation power islands. (a) S_{21} of isolation power islands. (b) Coupled noise at port 2.

reduced more than 90% on output port 2 by employing a strip of the rectangular EBG with a width of 4 cm and more than 75% by spiral EBG design with a width of 1.44 cm. In other words, the employment of spiral design leads to about 70% area reduction, but with a 15% decrease in time-domain noise suppression as a tradeoff.

Different feeding positions at $c = 12$ mm are also considered, which will cause more resonant modes within split planes. Here, the setup is the same as the previous case in Fig. 2(a) and (b). The full-wave simulator [14] is employed to analyze the coupled noise in the frequency domain between two isolation islands. The dotted line in Fig. 10(a) shows the simulation result without

Fig. 10. Reduction of coupling noise by rectangular EBG and spiral EBG structures between isolation power islands. (a) S_{21} of isolation power islands. (b) Coupling noise at port 2.

EBG structures. Significant coupling noise can be found at 2.3, 3.1, 3.8, and 4.6 GHz.

In this case, two kinds of cascaded spiral EBG are selected, one with $N = 1$ for high frequency and one with $N = 2$ for low frequency. The dimensions of the spiral EBG can be derived by using (2), (4), (5), and Fig. 6 as in the previous design. Good noise suppression can still be achieved with rectangular and spiral EBG structures, as is evident in Fig. 10(a). Fig. 10(b) shows the time-domain results. In this case, a similar setup is done as in the previous case. It can be seen that the spiral EBG structures can reduce noise by 75% on output port 2, but with much smaller total EBG size. Therefore, based on different resonant frequencies of radiated noise with different feeding positions, a specific spiral EBG can be designed for suppressing unwanted ground bounce noise.

B. Wideband Noise Suppression for Signal Line Across Slot

The signal propagating along a microstrip line over a slot on the power plane will also induce ground bounce noise [5], which will propagate within parallel plates. In this case, EBG structures can be used to suppress the ground bounce noise induced by a signal line. A typical multilayer structure is shown in Fig. 2(c), where the top layer is the signal plane, the middle

Fig. 11. Signal-line-crossing split power plane with embedded EBG structures for noise suppression. (a) Top view of stacked cascaded rectangular EBG structures. (b) Top view of stacked crossed rectangular EBG structures. (c) Side view of crossed rectangular EBG structures.

layer is the split power plane, and the bottom layer is the ground plane.

For example, consider the EBG-enhanced structure given in Fig. 11 with dimensions $a = 30$ mm, $b = 50$ mm, substrate thickness $t = 1.54$ mm, dielectric constant 4.4, and gapwidth $g = 1$ mm. A Gaussian voltage source with amplitude of 2 V and rising time of 100 ps launches onto the microstrip line at A. Furthermore, the voltage source is in series with an internal resistance of 50Ω , while on the other end the signal line is terminated with a matched load at B.

Since the slot-induced ground bounce propagates outward between the parallel plates, the combination of rectangular EBG structures deserves consideration. Two kinds of EBG arrangements are compared here. One is the traditional cascaded rectangular EBG structures shown in Fig. 11(a), and the other is the crossed rectangular EBG structures shown in Fig. 11(b). Based on the design guideline in Section II, two kinds of EBG structures with only two rows are used for suppressing two main resonant frequencies.

Fig. 12 shows the time-domain simulation results. The voltages at points A–D of Fig. 11 are compared among the crossed EBG, cascaded EBG, and the case with no EBG. It can be found

Fig. 12. Simulated waveforms at points A–D in Fig. 11 for signal line through split power plane with or without EBG structures.

that the presence of both EBG structures only have a little influence on the signal integrity of original signal at source A and received signal at B. However, it can successfully reduce the ground bounce at C and D as shown in Fig. 11(c) between power and ground planes. Cascaded EBG structures show different improvement at C and D because of the asymmetric arrangement, and the best reduction in ground bounce noise is about 45%. If crossed EBG structures are used, it can achieve about 62% ground bounce noise reduction compared with the case with no EBG. Hence, the crossed EBG structures can provide better noise reduction for omni directionally propagating slot-induced ground bounce. Similar conclusions can be derived for spiral EBG structures with different numbers of turns.

IV. EXPERIMENT VALIDATION

A two-layer PCB of two isolation islands is fabricated to investigate the coupling noise between the two split plates. Consider the structure shown in Fig. 2(a) and (b) with dimensions $a = 30$ mm, $b = 50$ mm, $c = 0$ mm, substrate thickness $t = 1.6$ mm, dielectric constant 4.4, and gapwidth $g = 1$ mm. Two kinds of two-row EBG structures with rectangular or spiral scheme are cascaded to enhance the noise-suppressing ability of the isolation islands. By using (2), (4), and (5) and the design diagram of Fig. 8, the widths of rectangular EBG structures are designed to be 8 and 12 mm and the widths of spiral ones to

Fig. 13. Comparison between simulated and measured results of: (a) rectangular- and (b) spiral-embedded split power planes in the frequency domain.

be 3.4 mm ($N = 1$) and 3.8 mm ($N = 2$). The simulated and measured waveforms will be compared in both the time and frequency domains to verify the better ground bounce noise reduction by EBG-enhanced split plane structures.

For the frequency-domain verification, the scattering parameters S_{21} are measured on a vector network analyzer R&S ZVB20. The comparisons with the simulated results of rectangular and spiral EBG structures are presented in Fig. 13. It can be seen that serious noise coupling occurs at some resonant frequencies. However, through the insertion of cascaded two-row EBG structures, both the simulated and measured results exhibit better than 20-dB improvement in the noise isolation at the two-frequency band gap, each over 1-GHz bandwidth. As a whole, the present EBG-enhanced split planes can provide ultra-wideband ground bounce noise suppression from dc to 5 GHz. This is validated by the good agreement between measurement and simulation results.

Fig. 14. Comparison between simulated and measured results of: (a) rectangular- and (b) spiral-embedded split power planes in the time domain.

For the time-domain measurement, the experimental verification is performed on a reflectometer TEK/CSA8000. A ramped step pulse of 0.5 V and rising time of approximately 50 ps is used as the excitation on port 1. The coupling noise can be measured from the TDT signal, which shows a peak-to-peak noise of about 23.8 mV in the absence of EBG structures. This means that the coupling noise by isolation islands for the present case may achieve about 9.5% of input signal. The simulated and measured waveforms of TDT signals with rectangular and spiral EBG layouts are both shown in Fig. 14. It is found that the coupled noise can be significantly suppressed by 81% and 64%, respectively. Good agreement is also noticed from the comparison between simulation and experimental results.

V. CONCLUSION

In this paper, an EBG-enhanced structure for ultra-wideband noise suppression on split power/ground planes and signal line

crossing slot is proposed, designed, examined, and validated. Using the concept of cascading EBG structures with different band-reject frequencies, the coupling noise between isolation islands can be significantly reduced. Compact size can also be achieved by spiral EBG structures with an increasing number of turns to save the occupied area, but with some relative bandwidth shrinkage as the tradeoff.

For ease and accuracy in the design of EBG structures, the modified inductance formula, the design chart of spiral EBG structures, and the minimum number of EBG rows are also presented. A systematic design procedure is established based on which the design of EBG structures for suppressing undesired frequencies becomes more convenient, without resorting to the time-consuming full-wave simulator.

REFERENCES

- [1] S. Radu and D. Hockanson, "An investigation of PCB radiated emission from simultaneous switching noise," in *IEEE Int. Electromagn. Compat. Symp.*, Aug. 1999, vol. 2, pp. 893–898.
- [2] S. Shahparnia and O. M. Ramahi, "Electromagnetic interference (EMI) reduction from printed circuit board (PCB) using electromagnetic bandgap structures," *IEEE Trans. Electromagn. Compat.*, vol. 46, no. 6, pp. 580–587, Nov. 2004.
- [3] Y.-J. Kim, H.-S. Yoon, S. Lee, G. Moon, J. Kim, and J.-K. Wee, "An efficient path-based equivalent circuit model for design, synthesis, and optimization of power distribution networks in multilayer printed circuit boards," *IEEE Trans. Adv. Packag.*, vol. 27, no. 1, pp. 97–106, Feb. 2004.
- [4] C. T. Wu and R. B. Wu, "Two-dimensional finite-difference time-domain method combined with open boundary for signal integrity issues between isolation islands," in *IEEE 11th Elect. Perform. Electron. Packag. Topical Meeting*, Oct. 2002, pp. 283–286.
- [5] C. T. Wu, G. H. Shiue, S. M. Lin, and R. B. Wu, "Composite effects of reflections and ground bounce for signal line through a split power plane," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 297–301, May 2002.
- [6] M. Xu and T. H. Hubing, "Estimating the power bus impedance of printed circuit boards with embedded capacitance," *IEEE Trans. Adv. Packag.*, vol. 25, no. 3, pp. 424–432, Aug. 2002.
- [7] S. Shahparnia and O. M. Ramahi, "Simultaneous switching noise mitigation in PCB using cascaded high-impedance surfaces," *Electron. Lett.*, vol. 40, pp. 98–100, Jan. 2004.
- [8] R. Abhari and G. V. Eleftheriades, "Metallo-dielectric electromagnetic bandgap structures for suppression and isolation of parallel-plate noise in high-speed circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 6, pp. 1629–1639, Jun. 2003.
- [9] T. Kamgaing and O. M. Ramahi, "A novel power plane with integrated simultaneous switching noise mitigation capability using high impedance surface," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 1, pp. 21–23, Jan. 2003.
- [10] S. Shahparnia and O. M. Ramahi, "Simple and accurate circuit models for high-impedance surfaces embedded in printed circuit boards," in *Proc. IEEE Antennas Propagat. Symp.*, Jun. 2004, vol. 4, pp. 3565–3568.
- [11] C. L. Wang, G. H. Shiue, and R. B. Wu, "EBG-enhanced split power planes for wideband noise suppression," in *Proc. IEEE 13th Elect. Perform. Electron. Packag. Topical Meeting*, Oct. 2005, pp. 61–64.
- [12] J. Lee, H. Kim, and J. Kim, "High dielectric constant thin film EBG power/ground network for broadband suppression of SSN and radiation emissions," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 8, pp. 505–507, Aug. 2005.
- [13] S. Shahparnia and O. M. Ramahi, "Miniaturized electromagnetic bandgap structures for ultra-wide band switching noise mitigation in high-speed printed circuit boards and packages," in *Proc. IEEE 13th Elect. Perform. Electron. Packag. Topical Meeting*, Oct. 2004, pp. 211–214.
- [14] High Frequency Structure Simulator. ver. 9.1, Ansoft, Pittsburgh, PA. [Online]. Available: www.ansoft.com
- [15] Microwave Studio. ver. 5.1, CST, Darmstadt, Germany [Online]. Available: www.cst.com

Chien-Lin Wang was born in Taipei, Taiwan, R.O.C., in 1982. He received the B.S. degree in electrical communication engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2004, and the M.S. degree from the Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan, R.O.C., in 2006.

His areas of interest are signal/power integrity and ground bounce suppression with EBG structure and analysis of interconnect electromagnetic problem in printed circuit boards.

Wei-Da Guo was born in Taoyuan, Taiwan, R.O.C., on September 25, 1981. He received the B.S. degree in communication engineering from the Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2003, and is currently working both the M.S. and Ph.D. degrees in communication engineering at National Taiwan University, Taipei, Taiwan, R.O.C.

His research interests include computational electromagnetics and signal/power integrity in the design of high-speed digital systems.

Guang-Hwa Shiue was born in Tainan, Taiwan, R.O.C., in 1969. He received the M.S. degree in electrical communication engineering from National Taiwan University of Science and Technology, Taipei, Taiwan, R.O.C., in 1997, and the Ph.D. degree in communication engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 2006.

He is currently a Teacher with the Electronics Department, Jin Wen Institute of Technology, Taipei, Taiwan, R.O.C. His areas of interest include numerical techniques in electromagnetics, microwave

planar circuits, signal/power integrity, and electromagnetic interference/compatibility for high-speed digital systems, and electrical characterization of system-in-package.

Ruey-Beei Wu (M'91–SM'97) received the B.S.E.E. and Ph.D. degrees from National Taiwan University, Taipei, Taiwan, R.O.C., in 1979 and 1985, respectively.

In 1982, he joined the faculty of the Department of Electrical Engineering, National Taiwan University, where he is currently a Professor and the Department Chair. He is also with the Graduate Institute of Communications Engineering, which was established in 1997. From March 1986 to February 1987, he was a Visiting Scholar with IBM, East Fishkill, NY. From

August 1994 to July 1995, he was with the Electrical Engineering Department, University of California at Los Angeles (UCLA). He became the Director of the National Center for High-performance Computing (1998–2000) and has served as the Director of Planning and Evaluation Division since November 2002, both under the National Science Council. His areas of interest include computational electromagnetics, transmission-line and waveguide discontinuities, microwave and millimeter-wave planar circuits, and interconnection modeling for computer packaging.