Gain-Enhancement Techniques for CMOS Folded Cascode LNAs at Low-Voltage Operations

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Abstract—In this paper, gain-enhancement techniques suitable for folded cascode low-noise amplifiers (LNAs) at low-voltage operations are presented. By employing a forward bias and a capacitive divider at the body of the MOSFETs, the LNA circuit can operate at a reduced supply voltage while maintaining an enhanced gain due to suppression of the negative impact of the body transconductance. In addition, a G_m -boosting stage is introduced to further increase the LNA gain at the cost of circuit linearity. Using a standard 0.18- μm CMOS process, two folded cascode LNAs are demonstrated at the 5-GHz band based on the proposed topologies. Consuming a dc power of 1.08 mW from a 0.6-V supply voltage, the LNA with the forward-body-bias technique demonstrates a gain of 10.0 dB and a noise figure of 3.37 dB. The measured $P_{1\text{dB}}$ and IIP₃ are -18 and -8.6 dBm, respectively. For the LNA with a G_m -boosting feedback, a remarkable gain of 14.1 dB gain is achieved with a dc power of 1.68 mW.

Index Terms—Body transconductance, folded cascode, forward body bias, G_m boosting, low-noise amplifiers (LNAs), low power, low voltage.

I. INTRODUCTION

THE increasing demand in personal wireless communications has motivated the development of fully integrated RF frontends in a CMOS process provided by commercial foundries. With the continuous shrinking of the feature size, superior high-frequency characteristics of the active devices have been demonstrated in deep-submicrometer CMOS technologies, facilitating RF integrated circuit (RFIC) designs at multigigahertz frequencies. Limited by the reliability issues in the gate oxide, the operating voltage of the MOSFETs progressively reduces with the device scaling. However, in order to sustain required noise margin and manageable leakage current for digital circuitry, the decrease in threshold voltage is not as significant. The insufficient voltage headroom has a strong impact on the performance of RF designs implemented in a conventional circuit topology. Consequently, research on low-voltage RFICs has attracted great attention and various circuit techniques have been proposed in the past few years [1]–[3].

Being widely utilized as the first active circuit in a receiver frontend, a low-noise amplifier (LNA) is a crucial component

Fig. 1. Circuit schematic of the conventional folded cascode LNA.

that predetermines the sensitivity and dynamic range in a wireless communication system. In order to satisfy the requirements for low-voltage operations, circuit techniques suitable for folded cascode LNAs are presented in this study. By employing the proposed forward-body-bias and G_m -boosting techniques, two LNA circuits were implemented in a standard 0.18- μm CMOS technology for demonstration, exhibiting enhanced RF performance at reduced supply voltage and power consumption.

This paper is organized as follows. Section II briefly introduces the circuit topology of conventional folded cascode LNAs. Sections III and IV describe the proposed circuit techniques and the design of two CMOS LNAs for low-voltage operations. Experimental results of the fabricated circuits are presented in Section V, while concluding remarks are provided in Section VI.

II. CONVENTIONAL FOLDED CASCODE LNA

With the unparalleled advantages in terms of gain, isolation, stability, and impedance matching, a cascode stage is considered one of the most widely used topologies for the implementation of LNA circuits at multigigahertz frequencies. However, with the stacking architecture of the common-source and common-gate transistors, relatively large bias voltage is required in the LNA design, and the performance degrades significantly as the supply voltage decreases. For low-voltage applications, a folded topology was proposed for cascode LNAs [4], [5]. Fig. 1 shows a simplified circuit schematic of the folded cascode LNA where M_1 and M_2 represent the first and second gain stages, respectively. In the circuit implementation, the impedance matching at input is achieved by L_1 and L_2 , while the network $L_4 - C_1$ is adopted for output matching. As the inductance L_3 resonates with the interstage parasitic capacitance at the frequencies of

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Fig. 2. Forward-body-bias technique in a triple-well CMOS process.

interest, the bias current for M_1 and M_2 is provided without introducing excessive loading to the gain stages.

Due to the absence of stacking gain stages, the operating voltage of the folded cascode LNA can be reduced by one transistor overdrive. Compared with other low-voltage LNA topologies [6]–[8], the folded cascode one possesses exclusive advantages in terms of amplifier linearity, noise figure, and bias stability. However, the inherently low gain is one of the major concerns, especially for applications where the current consumption is limited. In this study, gain-enhancement techniques are proposed for the folded cascode topology and high-gain LNAs are realized for low-voltage and low-power RF applications.

III. FOLDED CASCODE LNA WITH FORWARD BODY BIAS

A. Forward-Body-Bias Technique

For a standard CMOS process without the multiple gate–oxide option, the threshold voltage can be manipulated by the dc bias at the body terminal, adding one more degree of freedom in circuit designs. Typically, the threshold voltage of an n -channel MOSFET is given as [9]

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \quad (1)$$

where V_{SB} is the source-to-body voltage, V_{t0} is the threshold voltage for $V_{SB} = 0$, γ is a process-dependent parameter, and ϕ_F is a semiconductor parameter with a typical value in the range of 0.3–0.4 V [9]. Since a forward body bias effectively lowers the threshold voltage, the MOSFETs can operate at a reduced bias voltage while maintaining equivalent device characteristics in terms of gain, linearity, and noise figure.

It is noted that, as the forward body bias turns on the source-to-body junction of the MOSFET, a dc current flows across the junction with an exponential dependence on the body voltage, leading to additional power consumption and possibly latch-up failure. In order to prevent the excessive junction conduction, a current-limiting resistor R_B is included at the body terminal. Moreover, a capacitor C_B is inserted between the body and source terminals to suppress the negative influence from the body transconductance. Fig. 2 shows the implementation of the proposed forward-body-bias technique in a triple-well CMOS technology.

Fig. 3. Circuit schematic of the proposed LNA with forward body bias.

Fig. 4. Two-stage equivalent model for the folded cascode LNA.

B. Proposed LNA Topology

Fig. 3 shows the schematic of the proposed folded cascode LNA including the matching networks and bias circuits. To facilitate circuit design at a reduced supply voltage, the forward-body-bias technique is adopted for both M_1 and M_2 . The design consideration and circuit analysis are provided as follows.

1) *Gain*: For small-signal analysis, the proposed LNA is treated as a two-stage amplifier, and a simplified circuit model is illustrated in Fig. 4. In consideration of the gain and reflection coefficients at the frequency of interest, the maximum power transfer can be achieved by the conjugate matching conditions [10]

$$Z_S = Z_{IN,1}^* \quad (2)$$

$$Z_{OUT,1} = Z_{IN,2}^* \quad (3)$$

$$Z_{OUT,2} = Z_L^* \quad (4)$$

It is noted that, in conventional circuit implementations, the interstage node of the folded cascode LNA is considered low impedance, and the Miller effect of M_1 is insignificant. However, with reduced supply voltage and power consumption, it is no longer true, as the transconductance of the second stage M_2 is inherently low. Therefore, conjugate matching is adopted in

Fig. 5. Small-signal equivalent circuit of the common-source MOSFET with the forward-body-bias technique.

the circuit design to achieve maximum power transfer for enhanced gain.

In the design of LNA circuits, the gain is predetermined by the transconductance of the MOSFETs. Due to the use of the forward-body-bias technique, the transistors' threshold voltage is effectively reduced, leading to enhanced transconductance at low-voltage operations. On the other hand, with a sufficiently large current-limiting resistor R_B , the body of the transistor is considered floating at RF frequencies and a small-signal voltage v_{sb} develops between the body and source terminals. Therefore, the influence of the body transconductance g_{mb} has to be taken into account in the design of the individual gain stages.

The small-signal equivalent circuit of the common-source gain stage is shown in Fig. 5 where the gate-to-drain capacitance C_{gd} is neglected to simplify the analysis. For a floating-body MOS transistor, a small-signal voltage v_{sb1} is induced by the output swing due to the voltage divider established by parasitic capacitance C_{db1} and C_{sb1} . As the signals at the input and output are typically out of phase for a common-source stage, the small-signal current resulted from g_{mb1} is in the opposite direction to that from g_{m1} , leading to a degraded transconductance of the input stage due to the use of the forward-body-bias technique. To alleviate the negative impact of the body transconductance, a capacitor C_{B1} is adopted. Based on the equivalent circuit, the effective transconductance of the input stage is given by

$$G_{m1} \equiv \frac{I_{o1}}{V_{i1}} = \frac{g_{m1}}{\frac{g_{mb1}C_{db1} + j\omega C_{db1}(C_{sb1} + C_{B1})}{C_{db1} + (C_{sb1} + C_{B1})} \cdot Z_x + 1}. \quad (5)$$

Fig. 6. Small-signal equivalent circuit of the common-gate stage.

Typically, conjugate matching is required at the output of the common-source stage such that the LNA gain can be maximized. At the frequencies of interest, the load impedance Z_x is represented as an inductive element $j\omega L_x$, the magnitude of the effective transconductance is given in (6), shown at the bottom of this page, by neglecting the real part of Z_x for simplicity. For $(C_{B1} + C_{sb1}) \gg C_{db1}$, the expression in (6) is approximated by

$$|G_{m1}| = \frac{g_{m1}}{\sqrt{1 - (\omega/\omega_x)^2}} \approx g_{m1} \quad (7)$$

where

$$\omega_x = \frac{1}{\sqrt{L_x C_{db1}}}. \quad (8)$$

For circuit implementations, ω_x is much higher than the operating frequency and the effective transconductance is simply g_{m1} as the value of C_{B1} is sufficiently large.

The second stage of the folded cascode LNA is realized by a common-gate pMOS transistor and its small-signal equivalent circuit is shown in Fig. 6. Since the common-gate stage typically provides a positive voltage gain, in contrast with a common-source stage, the small-signal current resulted from g_{mb2} aligns with that from g_{m2} . However, a bypass capacitance C_{B2} is still adopted for optimum gain. Based on the equivalent circuit, the voltage gain of the second stage is given by (9), shown at the bottom of this page, at the operating frequency. For conjugate matching at the drain of M_2 , the load Y_y is inductive, indicating

$$|G_{m1}| = \frac{g_{m1}}{\sqrt{\left(1 - \frac{\omega^2 C_{db1}(C_{sb1} + C_{B1})L_x}{C_{db1} + (C_{sb1} + C_{B1})}\right)^2 + \left(\frac{\omega g_{mb1}C_{db1}L_x}{C_{db1} + (C_{sb1} + C_{B1})}\right)^2}} \quad (6)$$

$$|A_{v2}| \equiv \left| \frac{V_{o2}}{V_{i2}} \right| = \frac{\sqrt{\left(g_{m2} + g_{mb2} \frac{C_{db2}}{C_{db2} + (C_{sb2} + C_{B2})}\right)^2 + \left(\omega \frac{C_{db2}(C_{sb2} + C_{B2})}{C_{db2} + (C_{sb2} + C_{B2})}\right)^2}}{\sqrt{\left(g_{mb2} \frac{C_{db2}}{C_{db2} + (C_{sb2} + C_{B2})} + \text{Re}[Y_y]\right)^2 + \left(\omega \frac{C_{db2}(C_{sb2} + C_{B2})}{C_{db2} + (C_{sb2} + C_{B2})} + \text{Im}[Y_y]\right)^2}} \quad (9)$$

a negative value of $\text{Im}(Y_y)$. Therefore, the capacitance C_{B2} is chosen such that the gain of the second stage is enhanced.

2) *Linearity*: By taking the short-channel effects into account, the drain current of an n -channel MOSFET is given by [9]

$$I_D = \frac{1}{2} \cdot \frac{\mu_n C_{ox}(W/L)(V_G - V_t)^2}{1 + \theta \cdot (V_G - V_t)} = \frac{k_n}{2} \cdot \frac{(V_G - V_t)^2}{1 + \theta \cdot (V_G - V_t)} \quad (10)$$

where θ is the normal field mobility degeneration factor and μ_n is the carrier mobility. In order to investigate the circuit linearity of the folded cascode LNA, the drain current of M_1 is expressed by a Taylor series truncated at the third term as

$$i_{d1} \approx c_1 v_{gs1} + c_2 v_{gs1}^2 + c_3 v_{gs1}^3 \quad (11)$$

while the coefficients c_1 and c_3 can be obtained by the derivatives as

$$c_1 = \frac{\partial I_{D1}}{\partial V_{G1}} = \frac{k_{n1} V_{OD1}(2 + \theta \cdot V_{OD1})}{2(1 + \theta \cdot V_{OD1})^2} \quad (12)$$

$$c_3 = \frac{1}{3!} \cdot \frac{\partial^3 I_{D1}}{\partial V_{G1}^3} = \frac{-k_{n1} \theta}{2(1 + \theta \cdot V_{OD1})^4}. \quad (13)$$

Note that $V_{OD1} = V_{G1} - V_t$ represents the overdrive voltage of M_1 . As indicated in [11], the input 1-dB gain compression point $P_{in-1 \text{ dB}}$ is given by

$$\begin{aligned} P_{in-1 \text{ dB}} &\approx \frac{0.0725}{R_S} \left| \frac{c_1}{c_3} \right| \\ &\approx \frac{0.0725}{R_S \theta} \cdot V_{OD1} \cdot (2 + \theta V_{OD1}) \cdot (1 + \theta V_{OD1})^2 \end{aligned} \quad (14)$$

where R_S is the input resistance. For a folded cascode LNA, due to the concurrent operation, the linearity is mainly determined by the first stage instead of the multiple stages in a cascaded amplifier. As a result, the expression of $P_{in-1 \text{ dB}}$ in (14) is only for the input stage, providing an estimate of the amplifier linearity in the circuit design. According to (14), $P_{in-1 \text{ dB}}$ of the LNA circuit generally increases with the overdrive voltage. Due to the use of the forward-body-bias technique and inductive source degeneration, the proposed LNA is suitable for low-voltage operations without sacrificing the circuit linearity.

3) *Noise Figure*: Another important specification of the LNAs is the noise figure, which is strongly influenced by the design of the input stage. For a folded cascode topology with source degeneration, noise and power matching can be achieved simultaneously. To have a better understanding on the input matching, the equivalent circuit utilized for noise analysis is shown in Fig. 7, where v_{ns} and Z_{ns} are the Thevenin's equivalency of the source, and i_{ng}^2 and i_{nd}^2 represent mean-square values of the gate-induced and channel noise currents, respectively. Conventionally, the noise currents of a MOSFET are given by [12]

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \quad (15)$$

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \Delta f \quad (16)$$

Fig. 7. Small-signal equivalent circuit of the LNA input stage with noise current sources.

where δ and γ have typical values of 4/3 and 2/3, respectively. It is noted that g_g can be expressed as [12]

$$g_g = \frac{\omega^2 C_{gs1}^2}{5g_{d0}} \quad (17)$$

and g_{d0} is the zero-bias drain conductance. Assuming that the effect of g_{ds1} is negligible, the two-port noise parameters of the equivalent circuit can be derived. The noise resistance R_n , the minimum noise factor F_{min} and the optimum source impedance $Z_{opt,1}$ are given by [12], [13]

$$R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_{m1}} \quad (18)$$

$$F_{min} = 1 + \frac{2\omega}{\sqrt{5}\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \quad (19)$$

$$\begin{aligned} Z_{opt,1} &\approx j \frac{1}{\omega C_{gs1}} - j\omega L_2 \\ &+ \frac{\sqrt{\frac{\alpha^2 \delta}{5\gamma}(1 - |c|^2)}}{\omega C_{gs1} \left[\frac{\alpha^2 \delta}{5\gamma}(1 - |c|^2) + \left(1 + \sqrt{\frac{\alpha^2 \delta |c|^2}{5\gamma}} \right)^2 \right]} \end{aligned} \quad (20)$$

where $\alpha = g_{m1}/g_{d0}$ and $|c|$ is a correlation coefficient with a predicted value of 0.395 [12]. Based on the small-signal analysis, the input impedance $Z_{IN,1}$ at the gate of M_1 is approximated by

$$Z_{IN,1} \approx j\omega L_2 + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1} L_2}{C_{gs1}}. \quad (21)$$

From (20) and (21), the simultaneous power and noise matching is achieved if $Z_{opt,1}$ is the complex conjugate of $Z_{IN,1}$, resulting in

$$\frac{g_{m1} L_2}{C_{gs1}} = \frac{\sqrt{\frac{\alpha^2 \delta}{5\gamma}(1 - |c|^2)}}{\omega_0 C_{gs1} \left[\frac{\alpha^2 \delta}{5\gamma}(1 - |c|^2) + \left(1 + \sqrt{\frac{\alpha^2 \delta |c|^2}{5\gamma}} \right)^2 \right]}. \quad (22)$$

By properly choosing the device parameters to satisfy (22), the input stage of the LNA exhibits a noise factor of F_{min} while

Fig. 8. Simulated threshold voltage and leakage current versus R_B .

maintaining a maximum power gain and a low input return loss at the operating frequency ω_0 .

With the proposed topology for the folded cascode LNA, extra design issues have to be taken into account for the noise figure. As the forward bias turns on the source-to-body junction of the MOSFET, the shot noise associated with the current across the junction contributes to additional noise sources in the LNA operation. Furthermore, since the body terminal is connected to a forward bias voltage, the noise figure may increase due to the coupling of external noise and supply fluctuation through the body. To minimize the negative impact on the circuit performance, the resistance value of R_B has to be sufficiently large to suppress the forward junction current, while the low-pass property of the network $R_B - C_B$ can be properly designed to reject noise injection at the operating frequency.

C. Circuit Implementation

Based on the proposed folded cascode topology, a 5.2-GHz LNA is implemented using a standard 0.18- μm CMOS process. To facilitate the circuit design at a reduced supply voltage of 0.6 V, the device characteristics of the MOSFET under a forward body bias are first investigated. At various values of V_{B1} , the simulated junction leakage and equivalent threshold are shown in Fig. 8. With a current-limiting resistance of 12 k Ω and V_{B1} of 0.3 V, an effective threshold voltage of 0.45 V can be achieved while maintaining a junction leakage less than 0.05 μA .

In the LNA design, four on-chip inductors are employed for impedance-matching purposes. It is well known that the noise figure of the LNA is strongly influenced by the quality factor of L_1 , which locates in the series path at the input. On the other hand, the property of L_3 plays an important role in the LNA gain. The shunt inductor L_3 serves as an RF choke such that the small-signal current generated by M_1 is directed into the source of M_2 . In practice, the LNA gain is vulnerable to the shunt path resulted from the inductor losses. Therefore, in this particular design, the inductance values and the device layout for both L_1 and L_3 are optimized for Q factors, leading to enhanced LNA performance at reduced supply voltage and power consumption.

In the circuit analysis, the capacitors C_{B1} and C_{B2} are utilized to maximize the gains of the common-source and common-gate stages, respectively. To provide useful design

Fig. 9. Simulated $|G_{m1}|$ versus the capacitance ratio with $V_{B1} = 0.3$ V. Fig. 10. Simulated $P_{in-1\text{ dB}}$ versus V_{G1} for various values of V_{B1} with $V_{B2} = 0.3$ V.

guidelines for the capacitance value of C_{B1} , circuit simulations were performed and the effective transconductance of the input stage at the 5-GHz frequency band is illustrated in Fig. 9. From the simulation results, as C_{B1} becomes four times as large as C_{db1} , $|G_{m1}|$ nearly saturates to a value of 17.5 mA/V. To have sufficient margin for process variation and device mismatch, the capacitance ratio is 10 in this particular design, leading to a gain enhancement of 1.4 dB at the center frequency.

As the threshold is effectively reduced by the forward body bias, the LNA exhibits reasonable linearity at low-voltage operations. Fig. 10 shows the simulated $P_{in-1\text{ dB}}$ versus the gate bias of M_1 for various values of V_{B1} . As predicted in (14), $P_{in-1\text{ dB}}$ increases with the overdrive voltage for MOS transistors operating in saturation. It is also noted that the linearity increases at low gate voltage as the transistors operate in weak inversion. Therefore, the tradeoff between gain and linearity has to be taken into account in determining the bias voltage of the LNA circuit.

Due to the use of the RC network at the body terminal, the influence on the LNA noise figure is investigated by circuit simulations. Fig. 11 depicts the simulated noise figure versus the current-limiting resistances. To effectively suppress the shot noise due to the forward bias at the source-to-body junctions, the resistance values, especially for R_{B1} , have to be sufficiently large. According to the simulation results, the impact on the noise figure can be minimized for R_{B1} and R_{B2} larger than 5 k Ω .

Fig. 11. Simulated noise figure versus resistance values with $V_{B1} = V_{B2} = 0.3$ V.

TABLE I
CIRCUIT PARAMETERS OF THE 5.2-GHz FOLDED CASCODE LNA

Devices	Design Values
M_1	100 $\mu\text{m}/0.18 \mu\text{m}$
M_2	125 $\mu\text{m}/0.18 \mu\text{m}$
L_1	5.7 nH
L_2	0.8 nH
L_3	2.7 nH
L_4	3.8 nH
C_1	0.15 pF
C_{B1}	1.3 pF
C_{B2}	8.2 pF
R_{B1}, R_{B2}	10 k Ω
V_{B1}	0.3 V
V_{B2}	0.3 V

By taking the design considerations into account, the circuit parameters of the 5.2-GHz folded cascode LNA are tabulated in Table I.

IV. LNA WITH G_m -BOOSTING TECHNIQUE

A. G_m -Boosting Technique

Based on the proposed circuit topology, a G_m -boosting technique can also be incorporated in the LNA design to further increase the transconductance of the MOSFETs at low bias voltage. A conceptual illustration of the G_m -boosting technique [14] is shown in Fig. 12. For a common-gate MOSFET, as depicted in Fig. 12(a), the transconductance is typically specified by the small-signal circuit parameter g_m . By introducing an inverted replica signal with an amplitude n times as large at the gate terminal, the gate-to-source voltage is increased by a factor of $(1 + n)$, as illustrated in Fig. 12(b). Consequently, the transconductance is thus boosted for enhanced circuit performance. It is noted that the replica signal can be either generated by a transformer or provided by an amplifier circuit. In this study, an inverting amplifier stage is adopted for the replica signal such that the LNA gain can be maximized at reduced supply voltage and power consumption.

Fig. 12. Transistor: (a) without and (b) with the G_m -boosting technique.

Fig. 13. (a) Circuit schematic of the folded cascode LNA with the G_m -boosting technique. (b) Feedback stage for G_m boosting.

B. Proposed Circuit Topology

Fig. 13(a) shows the circuit schematic of the folded cascode LNA with the G_m -boosting technique at the common-gate stage. In order to provide an inverted replica at the gate of M_2 , a feedback loop with an additional common-source stage M_3 , as shown in Fig. 13(b), is employed. Assuming that the voltage gain provided by the feedback stage M_3 is $-A_3$, the effective transconductance of the common-gate stage becomes $g_{m2}(1 + A_3)$. For small-signal analysis purposes, the output of M_3 is modeled by a simplified equivalent circuit, as depicted in Fig. 13(b), and the effective voltage gain is given by

$$A_3 \approx - \frac{g_{m3} R_2 L_5}{C_{g2}} \cdot \frac{1}{\left(\frac{L_5}{C_{g2}} - \frac{1}{\omega^2 C_3 C_{g2}} \right) + j R_2 \left(\omega L_5 - \frac{C_3 + C_{g2}}{\omega C_3 C_{g2}} \right)} \quad (23)$$

Fig. 14. Simulated: (a) gain, (b) noise figure, and (c) $P_{in-1\text{ dB}}$ of the LNA versus the design parameters of the feedback stage M_3 .

By choosing the operating frequency ω_0 as

$$\omega_0 = \sqrt{\frac{C_3 + C_{g2}}{L_5 C_3 C_{g2}}} \quad (24)$$

the gain for the feedback stage M_3 is simply

$$A_3 = -g_{m3} R_2 \left(1 + \frac{C_{g2}}{C_3} \right). \quad (25)$$

As indicated in (25), A_3 is governed by the transconductance of M_3 , the load resistance, and the capacitance ratio. For low-power circuit designs, it is desirable to minimize the dc current of M_3 . Therefore, the required gain of the feedback stage is achieved by the aspect ratio of M_3 and the load resistance at

Fig. 15. Simulated stability factor and gain with the sweep of R_2 .

Fig. 16. Simulated stability factor and $|S_{21}|$ with $R_2 = 1$ k Ω .

TABLE II
CIRCUIT PARAMETERS OF THE G_m -BOOSTED LNA

Devices	Design Values
M_1	100 $\mu\text{m}/0.18$ μm
M_2	117.5 $\mu\text{m}/0.18$ μm
M_3	50 $\mu\text{m}/0.18$ μm
L_1	4.9 nH
L_2	1.0 nH
L_3	2.7 nH
L_4	4.1 nH
L_5	2.1 nH
C_1	0.12 pF
C_2	2.7 pF
C_3	0.7 pF
R_{B1}	10 k Ω
R_2	1 k Ω
V_{B1}	0.2 V

a specified current consumption. Once the design parameters of M_3 and R_2 are determined, the values of C_3 and L_5 are chosen such that (24) satisfies.

C. Design Considerations

By incorporating the G_m -boosting technique in the proposed folded cascode topology, an LNA is designed and implemented at the 5-GHz band for demonstration. In order to investigate the influence of the feedback stage on the LNA performance, circuit simulations were performed and the results are shown in Fig. 14.

Fig. 17. Microphotograph of the fabricated folded cascode LNA.

Fig. 18. (a) Measured and simulated $|S_{21}|$ and noise figure. (b) $|S_{11}|$ and $|S_{22}|$ of the folded cascode LNA.

For a load resistance R_2 of 1 k Ω , the LNA gain increases monotonically with the aspect ratio and gate bias of M_3 due to the enhanced effective transconductance of the common-gate stage. In addition, the noise figure of the LNA is also influenced by the feedback loop established for G_m boosting. As for the linearity, the concurrent operation of the gain stages M_1 and M_2 no longer exists due to the use of the G_m -boosting stage. Therefore, the LNA has to be treated as a cascaded amplifier and $P_{in-1\text{ dB}}$ decreases accordingly. For circuit implementations, the tradeoff between gain and linearity is essential in determining the design parameters of the feedback loop in the proposed LNA topology.

Fig. 19. Measured: (a) $P_{in-1\text{ dB}}$ and (b) IIP₃ of the folded cascode LNA.

Since the proposed G_m -boosting technique is considered a positive feedback, the circuit stability is also an important issue and special care has to be taken. For given aspect ratio and gate bias of M_3 , the simulated gain and stability factor versus the load resistance are demonstrated in Fig. 15. It is clear that, at the center frequency, the stability factor degrades as the gain of the feedback stage increases. To ensure the circuit stability ($K > 1$) at all frequencies, a load resistance of 1 k Ω is finally employed in this particular design, while the simulated $|S_{21}|$ and stability factor versus frequency are shown in Fig. 16. The circuit parameters of the G_m -boosted folded cascode LNA are summarized in Table II.

V. EXPERIMENTAL RESULTS

Using a 0.18- μm CMOS process, two folded cascode LNAs were implemented at the 5-GHz frequency band for demonstration. In this particular technology, the threshold voltage of the nMOS and pMOS transistors are approximately 0.5 V without the body effect. As for the on-chip passive components, AlCu metallization layer of 2- μm thickness is available for inductors while a metal-insulator-metal structure with oxide intermetal dielectric is utilized for capacitors. The RF performance of the fabricated circuits was characterized by on-wafer probing.

Based on the circuit topology presented in Fig. 3, a folded cascode LNA is realized at a center frequency of 5.2 GHz. Fig. 17 shows a microphotograph of the fabricated circuit with a chip area of $0.85 \times 0.83\text{ mm}^2$ including the pads. Operated at a supply voltage of 0.6 V, the LNA consumes a dc power of 1.08 mW.

Fig. 20. Microphotograph of the fabricated folded cascode LNA with the G_m -boosting technique.

Fig. 21. (a) Measured and simulated $|S_{21}|$ and noise figure. (b) $|S_{11}|$ and $|S_{22}|$ of the folded cascode LNA with the G_m -boosting stage.

The simulated and measured small-signal characteristics are depicted in Fig. 18, indicating a gain of 10.0 dB and a noise figure of 3.37 dB at 5.2 GHz. With the on-chip matching networks, the input and output ports are matched to $50\ \Omega$, and the measured $|S_{11}|$ and $|S_{22}|$ are -13.4 and -10.6 dB, respectively. In addition, the large-signal behavior of the fabricated LNA is evaluated and the results are demonstrated in Fig. 19. The measured $P_{in-1\text{ dB}}$ and IIP_3 are -18 and -8.6 dBm, respectively.

By incorporating the proposed G_m -boosting stage, another folded cascode LNA is also implemented at the same frequency band. The microphotograph of the fabricated circuit is shown

Fig. 22. Measured: (a) $P_{in-1\text{ dB}}$ and (b) IIP_3 of the fabricated folded cascode LNA with the G_m -boosting stage.

TABLE III
LNA PERFORMANCE AT VARIOUS GATE BIAS FOR THE FEEDBACK STAGE

	Unit	$V_{G3}=0.56\text{ V}$	$V_{G3}=0.58\text{ V}$	$V_{G3}=0.60\text{ V}$
P_{DC}	mW	1.47	1.57	1.68
$ S_{21} $	dB	11.6	12.9	14.1
NF	dB	4.15	3.84	3.65
IIP_3	dBm	-15.3	-16.1	-17.1

in Fig. 20 and the chip size measures $0.97 \times 0.80\text{ mm}^2$. Biased at a supply voltage of 0.6 V, the LNA consumes a dc power of 1.68 mW. The simulated and measured small-signal characteristics are illustrated in Fig. 21, indicating a gain of 14.1 dB and a noise figure of 3.65 dB at a center frequency of 5 GHz. On the other hand, the large-signal properties of the LNA are evaluated by its $P_{in-1\text{ dB}}$ and IIP_3 . Fig. 22 shows the measurement results with a $P_{in-1\text{ dB}}$ of -25 dB and an IIP_3 of -17.1 dB. It is noted that, in the proposed LNA topology, the tradeoff between gain and linearity can be realized by adjusting the gain of the feedback stage. As the gate bias of M_3 sweeps from 0.56 to 0.60 V, the measured LNA performance in terms of gain, noise figure, and IIP_3 are tabulated in Table III, featuring a tuning mechanism for the circuit operation. Finally, Table IV summarizes the performance of the fabricated LNAs along with results from previously published works [3]–[5] for comparison. It is clear that, with the proposed circuit techniques, enhanced LNA performance is demonstrated exclusively for low-voltage and low-power RF applications.

TABLE IV
PERFORMANCE COMPARISON OF LOW-VOLTAGE AND LOW-POWER LNAs

	Unit	This Work	This Work	[3]	[4]	[5]
Technology	—	0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS	90-nm CMOS
Frequency	GHz	5.2	5.0	5.0	5.8	5.5
Supply Voltage	V	0.6	0.6	0.6	1.0	0.7
DC Power	mW	1.08	1.68	0.9	22.2	12.5
Power Gain	dB	10.0	14.1	9.2	13.2	7.0
Noise Figure	dB	3.37	3.65	4.5	2.5	2.88
$ S_{11} $	dB	-13.4	-12.7	-12	-5.3	-7.1
$ S_{22} $	dB	-10.6	-14.0	-21	-10.3	-12.3
P_{in-1dB}	dBm	-18	-25	-27	-14	-9
IIP_3	dBm	-8.6	-17.1	-16	—	—
						-7.25

VI. CONCLUSION

In this study, circuit techniques are proposed for CMOS LNA designs. By incorporating a body-bias network with a G_m -boosting feedback in the circuit topology, enhanced gain can be achieved for folded cascode LNAs at reduced supply voltage and power consumption. Using a 0.18- μ m CMOS process, two LNAs were successfully implemented at the 5-GHz frequency band for demonstration. The proposed techniques are well suited for low-voltage and low-power RF applications at multigigahertz frequencies.

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