A 20-Gb/s 1 : 2 Demultiplexer With Capacitive-Splitting Current-Mode-Logic Latches

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Abstract—This paper presents a high-speed 1:2 demultiplexer (DEMUX) implemented in a 0.18- μm CMOS process. By employing a capacitive-splitting architecture for the current-mode-logic latches, a significant speed improvement is achieved in the proposed DEMUX. Provided a $2^{23} - 1$ pseudo-random bit sequence from the pattern generator, the fabricated circuit operates at an input data rate up to 20 Gb/s. The fully integrated DEMUX consumes a dc power of 150 mW from a 2-V supply voltage.

Index Terms—Bandwidth enhancement, capacitive-splitting latches, current-mode-logic (CML), demultiplexers (DEMUX), high-speed flip-flops, inductive peaking, optical-fiber communications.

I. INTRODUCTION

IN THE receiver frontend of an optical-fiber communication system, the demultiplexer (DEMUX) is an essential building block, which deserializes a high-speed data stream into several lower speed parallel data outputs. Owing to the increasing demands on the bandwidth for data transmissions, DEMUX integrated circuits operating at very high speed are required. In conventional circuit implementations, the maximum operation speed of such circuits is limited by the cutoff frequency (f_T) of the transistors. Therefore, III–V compound semiconductors and SiGe technologies were preferred for applications at a data rate beyond 10 Gb/s [1], [2].

With recent advances in the fabrication technologies, CMOS devices demonstrate a great potential for the high-speed circuit designs. Due to the reduced parasitics and enhanced transconductance from the device scaling, deep-submicrometer CMOS transistors with a cutoff frequency over 100 GHz were reported [3]. Based on state-of-the-art process technologies, a 1 : 2 DEMUX in 120-nm CMOS [4] and a 1 : 4 DEMUX in 90-nm CMOS [5] have been fabricated to operate at a data rate of 40 Gb/s. However, for a cost-efficient process such as the 0.18- μm CMOS, the highest data rate demonstrated for the DEMUX circuits is limited within 10 Gb/s [6], [7]. In this paper, capacitive-splitting architectures, which were originally developed for broadband amplifiers, are proposed for the high-speed latches to alleviate the speed limitations caused

Fig. 1. Cascaded stages with shunt-peaking inductance for bandwidth enhancement.

by the finite cutoff frequencies of the transistors. By employing the proposed technique, a fully integrated DEMUX operating at a data rate of 20 Gb/s is presented using a standard 0.18- μm CMOS process.

The remainder of this paper is organized as follows. Section II describes the proposed capacitive-splitting architectures for high-speed latches. The design and experimental results of the 1 : 2 DEMUX are presented in Sections III and IV, respectively. Finally, a conclusion is given in Section V.

II. CAPACITIVE-SPLITTING CML LATCHES

For high-speed DEMUX circuits, the highest input data rate is typically limited by the maximum operation speed of the master-slave flip-flops (MS-FFs), especially in CMOS designs. Conventionally, an MS-FF is composed of two cascaded static latches, and current-mode-logic (CML) stages with a series-gated topology [4] are widely used for the implementation of the high-speed latches. In order to overcome the speed limitations, bandwidth enhancement techniques, which were originally developed for broadband amplifiers, are investigated for the CMOS DEMUX circuits.

A. Circuit Architectures for Bandwidth Enhancement

In the design of conventional cascaded amplifiers with resistive loads, the bandwidth is primarily limited by the RC time constant of the individual stages. A widely used technique to enhance the bandwidth of such circuits is to employ the shunt-peaking inductors [8] in series connection with the resistive loads, as shown in Fig. 1. As the peaking inductance resonates with the nodal capacitance in the vicinity of the rolloff frequency, an extended bandwidth is demonstrated. For ultra-wideband applications, another effective technique is proposed to further boost the amplifier bandwidth by the capacitive-splitting

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Fig. 2. Capacitive-splitting architectures. (a) NE termination topology. (b) FE termination topology.

architecture [9]–[11]. With the series inductance inserted in between the cascaded stages to separate the capacitive loadings, wideband characteristics can be achieved.

In order to perform a systematic analysis on the bandwidth enhancement techniques, two simplified circuit models derived from the capacitive-splitting amplifiers are illustrated in Fig. 2, where C_1 and C_2 represent the output capacitance of the previous stage and the input capacitance of the following stage, respectively, and L_s is the series inductance, which separates the capacitive loadings C_1 and C_2 . Note that the major distinction between these two capacitive-splitting architectures lies in where the resistive-load branch is located. In the circuit model, as depicted in Fig. 2(a), the resistive-load branch is placed at the same node as C_1 , referred to as the near-end (NE) termination network. On the other hand, the far-end (FE) termination network, as shown in Fig. 2(b), places the loading branch on the side of C_2 . Even with the similarity in the capacitive-splitting architectures, very different circuit characteristics in terms of the frequency and step responses are demonstrated, especially when C_1 and C_2 are not evenly separated. Therefore, both capacitive-splitting architectures are investigated for the design of the high-speed CML latches.

B. Frequency and Step Response Analysis

Based on the simplified circuit models in Fig. 2, the transfer functions of the capacitive-splitting architectures are derived to evaluate the frequency and step response of the systems. For the NE and FE networks, the transfer functions can be expressed as

$$H_{\text{NE}}(s) = \left(\frac{V_{\text{out}}}{I_D} \right)_{\text{NE}} = - \frac{L_p \cdot s + R_L}{A \cdot s^4 + B \cdot s^3 + C_{\text{NE}} \cdot s^2 + D \cdot s + 1} \quad (1)$$

$$H_{\text{FE}}(s) = \left(\frac{V_{\text{out}}}{I_D} \right)_{\text{FE}} = - \frac{L_p \cdot s + R_L}{A \cdot s^4 + B \cdot s^3 + C_{\text{FE}} \cdot s^2 + D \cdot s + 1} \quad (2)$$

where

$$A = L_p L_s C_1 C_2$$

$$B = R_L L_s C_1 C_2$$

$$C_{\text{NE}} = L_p (C_1 + C_2) + L_s C_2$$

$$C_{\text{FE}} = L_p (C_1 + C_2) + L_s C_1$$

$$D = R_L (C_1 + C_2).$$

From (1) and (2), both networks can be characterized as fourth-order systems, which only differ from each other by one coefficient in the denominator. Theoretically, the poles of the systems can be analytically derived, but the expressions become too complicated to provide any useful insight for circuit design. Consequently, numerical and conceptual analyses are instead performed.

Before the analysis, it is noted that the transfer functions $H_{\text{NE}}(s)$ and $H_{\text{FE}}(s)$ are identical when $C_1 = C_2$. Nevertheless, this is generally not the case in practical designs since the drain capacitance (C_1) is smaller than the gate capacitance (C_2) in typical CMOS cascaded stages. For simplicity, the assumption $C_2 = 2C_1$ is employed as a special case. The first analysis is to illustrate the impact of the inductance ratio, which is defined as $m = L_s/L_p$, on the frequency responses. In both networks, the shunt inductance L_p is selected to provide a maximum flat frequency response as is the case in conventional shunt-peaking topology [8]

$$L_p = 0.41 \times R_L^2 C_L \quad (3)$$

where R_L is the load resistance, and $C_L = C_1 + C_2$ represents the total capacitance. With realistic inductor models, Fig. 3(a) and (b) shows the frequency responses of the NE and FE networks, respectively, with various m . It is observed from Fig. 3(a) and (b) that an additional high-frequency resonance and gain peaking take place due to the existence of L_s . As m increases, the resonant frequency moves toward the lower frequency band, while the midband gain recession diminishes. Therefore, with a proper selection of m , the -3 -dB bandwidth can be pushed beyond the high-frequency resonance, leading to an enhanced bandwidth with reasonable gain flatness in the passband. Fig. 4 depicts the frequency responses of the proposed capacitive-splitting architectures with the maximum achievable bandwidth. It is evident that the FE network outperforms its NE counterpart in terms of the bandwidth at the expense of excessive gain peaking in the vicinity of the rolloff frequency.

In order to have a better understanding of the distinction in the frequency responses between these two networks, behavior illustrations, as presented in [10], are provided. In the NE network, as shown in Fig. 5(a), the series connection of L_s and C_2 first resonates at $\omega_{1,\text{NE}}$, resulting in gain roll-up in the frequency response. The gain reaches a maximum value when the

Fig. 3. Simulated frequency responses with various inductance ratio m for the: (a) NE topology and (b) FE topology. ($\omega_0 = (R_L C_L)^{-1}$).

Fig. 4. Simulated frequency responses of the proposed capacitive-splitting architectures with the maximum achievable bandwidth. ($\omega_0 = (R_L C_L)^{-1}$).

π -network ($C_1 - L_s - C_2$) resonates at $\omega_{2,NE}$. Due to the high impedance demonstrated by the π -network, the current I_{in} is

forced to flow through R_L and L_p , and the gain peaking is estimated by

$$\left| \frac{V_{out}}{I_{in}} \right|_{NE} = R_L \sqrt{1 + (\omega_{2,NE} L_p / R_L)^2}. \quad (4)$$

At frequencies beyond $\omega_{2,NE}$, the π -network can be treated as an equivalent capacitance $C_{eq,NE}$. Consequently, the third resonant frequency $\omega_{3,NE}$ is determined by the inductance L_p and the capacitance $C_{eq,NE}$. As for the FE network, similar illustrations are presented in Fig. 5(b). The first resonance, which is determined by L_p and C_2 , takes place at $\omega_{1,FE}$. The high impedance provided by the parallel resonator forces the current I_{in} to charge the capacitance C_1 . At frequencies higher than $\omega_{1,FE}$, the parallel resonator becomes capacitive and is modeled by a shunt resistance and a shunt capacitance as

$$R_{eq,FE} = R_L + \frac{\omega^2 L_p^2}{R_L} \quad (5)$$

$$C_{eq,FE} = \frac{\omega^2 L_p^2 C_2 + R_L^2 C_2 - L_p}{R_L^2 + \omega^2 L_p^2}. \quad (6)$$

At the second resonant frequency $\omega_{2,FE}$, L_s and $C_{eq,FE}$ act as a short circuit to absorb the current I_{in} , leading to a gain roll-up in the frequency response. The gain roll-up peaks when the π -network ($C_1 - L_2 - C_{eq,FE}$) resonates. From (5) and (6), the resonant frequency and associated gain peaking can be expressed as

$$\begin{aligned} \omega_{3,FE} &= \frac{1}{2} \sqrt{\frac{C_1 + C_2}{L_s C_1 C_2} + \frac{1}{L_p C_2} + \sqrt{\left(\frac{C_1 + C_2}{L_s C_1 C_2} + \frac{1}{L_p C_2} \right)^2 - 4}} \end{aligned} \quad (7)$$

$$\begin{aligned} \left| \frac{V_{out}}{I_{in}} \right|_{FE} &= R_L \left(1 + \frac{\omega_{3,FE}^2 L_p^2}{R_L^2} \right). \end{aligned} \quad (8)$$

From the above analysis, two major differences between the proposed capacitive-splitting architectures are observed. First, the gain peaking occurs at the second resonance frequency in the NE network, while it takes place at the third resonant frequency in the FE network. Secondly, as predicted in (4) and (8), the FE network exhibits more severe gain peaking than the NE network does. As a result, the FE network can extend the -3 -dB bandwidth more effectively, which shows good agreement with the simulation results in Fig. 4.

Thus far, the analysis of the frequency responses are based on the assumption $C_2 = 2C_1$, which is a valid approximation for most cases in cascaded amplifiers. However, in the designs of high-speed digital circuits such as CML latches, the behavior of both networks with C_2 several times larger than C_1 must be investigated. Provided a fixed total capacitance C_L , simulated frequency responses for both circuit topologies with various capacitance ratio $k = C_2/C_1$ are illustrated in Fig. 6. In the NE network, the third resonant frequency increases with a

Fig. 5. Behavior illustrations of the capacitive-splitting architectures. (a) NE topology. (b) FE topology.

Fig. 6. Simulated frequency responses with various capacitance ratio (C_2/C_1) for the: (a) NE topology and (b) FE topology ($\omega_0 = (R_L C_L)^{-1}$).

diminishing gain peaking as k increases. On the other hand, the gain peaking and rolloff frequency of the FE network increase with k . From the numerical analysis performed above, a

conclusion can be made that, though the capacitive-splitting architecture with the FE topology is advantageous for bandwidth enhancement, the excessive gain peaking in the frequency re-

Fig. 7. Absolute root locus for the capacitive-splitting architectures as the capacitance ratio k increases.

Fig. 8. Simulated step responses of the NE and FE capacitive-splitting architectures for: (a) $k = 2$ and (b) $k = 4$.

sponse is undesirable in practical circuit designs, especially for high-speed latches with a large capacitance ratio.

To further evaluate the influence of the capacitance ratio k on the system behavior, the root locus and step response of both capacitive-splitting architectures are characterized. Provided that the total capacitance C_L and the inductance ratio m are fixed, the absolute root locus for both proposed topologies with an increasing capacitance ratio k are shown in Fig. 7. For $k = 1$, the total capacitance C_L is evenly distributed between C_1 and C_2 , leading to an identical characteristic equation for both architectures. As k increases, two poles move with decreasing σ , while

Fig. 9. Circuit schematic of the capacitive-splitting CML latches with the: (a) NE topology and (b) FE topology.

Fig. 10. Block diagram of the 1:2 DEMUX.

the other two poles move with increasing σ . Note that, in the FE network, the poles with smaller σ locate in close proximity to the $j\omega$ axis, especially when k becomes large, resulting in a reduced damping factor and an enhanced tendency of oscillation. In order to verify the observations, simulated step responses of

Fig. 11. Simulated: (a) output jitter and (b) eye-opening improvement factor of the capacitive-splitting CML latch with various L_p and m .

Fig. 12. Simulated output eye diagrams of the high-speed latches with: (a) conventional CML stage, (b) shunt-peaking inductance, (c) NE capacitive-splitting topology, and (d) FE capacitive-splitting topology.

the capacitive-splitting architectures with various k are shown in Fig. 8. As indicated in the plots, the FE network exhibits a faster transition due to the extended bandwidth. However, the output ringing and settling time become unacceptable when a large capacitance ratio is required.

C. Capacitive-Splitting High-Speed CML Latches

Based on the concept of the capacitive-splitting technique for bandwidth enhancement, two CML latches are proposed. Fig. 9(a) and (b) illustrates the circuit schematics with the NE

and FE topology, respectively. Due to the existence of the cross-coupled pair for data storing and the input capacitance of the following stage, C_2 is typically larger than C_1 by a factor of 4 in practical CML latch circuits. Although it is more effective to achieve an extended bandwidth by using the FE topology, the severe gain peaking near the rolloff frequency and the reduced damping factor are not desirable for high-speed latch operations. Even if the oscillation is prevented by selecting the circuit parameters carefully or deliberately adding a large series resistance along with L_s , larger ringing and long settling time

Fig. 13. Circuit schematic of the differential output buffer.

Fig. 14. Microphotograph of the fabricated 1 : 2 DEMUX.

would introduce excess intersymbol interference (ISI), leading to a significant degradation in the quality of the output eye diagram for high-speed data transmission. As a result, the NE network is adopted for the circuit implementation.

III. DESIGN OF 1 : 2 DEMUX

Fig. 10 shows the block diagram of the 1 : 2 DEMUX, which is composed of two MS-FFs and two output buffers. In order to sample the data stream provided at the input, a half-rate clock is applied to both of the MS-FFs with inverted phases. The outputs of the MS-FFs are buffered by a two-stage differential amplifier to drive the external 50- Ω load of the testing instruments.

The design of the capacitive-splitting MS-FF starts with the circuit parameters of the CML latches. In consideration of the specifications including the voltage gain, output swing, and gate delay, a load resistance of 100 Ω is employed and realized by polysilicon resistors in this particular design. The tail current is selected to provide an output voltage swing of 600 mV_{pp} for sufficient signal-to-noise ratio. Once the tail current is determined, the transistor size of the tracking stage M_1 – M_2 is optimized for the switching speed. In order to achieve high-speed operations,

Fig. 15. Measurement setup for the DEMUX circuit.

Fig. 16. Re-timed singled-ended eye diagram at 13 Gb/s with $2^{31} - 1$ PRBS input. (horizontal scale: 20 ps/div., vertical scale: 50 mV/div.).

Fig. 17. Output singled-ended eye diagram with an input data rate of 20 Gb/s (horizontal scale: 50 ps/div., vertical scale: 50 mV/div.).

the capacitance contributed by the cross-coupled pair M_3 – M_4 has to be minimized. Therefore, the transistor size of M_3 and M_4 is chosen such that the loop gain of the latch stage is slightly larger than unity to ensure the latch function. Finally, the clock switching pair M_5 – M_6 with a large transistor size is used for better sensitivity.

After determining the circuit parameters of the CML latches, the capacitive-splitting architecture is constructed by incorporating the inductors into the design. Since both frequency- and time-domain characteristics are strongly influenced by the capacitive-splitting architecture, careful attention is required in the selection of L_p and L_s . In order to optimize the circuit performance, simulated output jitter and eye-opening improvement factors with various values of L_p and m are demonstrated in

TABLE I
PERFORMANCE SUMMARY OF THE HIGH-SPEED CMOS DEMUX

Ref	[6]	[7]	[12]	[4]	[5]	[13]	This
Technology	0.18- μ m CMOS	0.18- μ m CMOS	0.12- μ m SOI	0.13- μ m CMOS	90-nm CMOS	0.13- μ m CMOS	0.18- μ m CMOS
Function	1:8	1:16	1:4	1:2	1:4	1:4	1:2
Maximum Data Rate	10 Gb/s	10 Gb/s	30 Gb/s	40 Gb/s	40 Gb/s	20 Gb/s	20 Gb/s
Supply	2 V	1.8 V	2 V	1.5 V	1.2 V	1.2 V	2 V
P_{diss}	102 mW	-	204 mW	108 mW	62 mW	210 mW	150 mW

Fig. 11(a) and (b), respectively. Note that the simulation results are based on a 20-Gb/s $2^7 - 1$ pseudorandom bit sequence (PRBS), while the eye-opening improvement factor is the vertical eye opening normalized to that of a conventional CML latch without any inductors. In this design, a 0.45-nH shunt-peaking inductance L_p is employed. As indicated in Fig. 11(a), output jitter reaches a minimum value of 0.01 unit interval (UI) with $m = 2.8$, and increases as $m > 2.8$. This is mainly due to the nonconstant group delay, which introduces excess ISI. However, in consideration of the rise and fall time at the output, an inductance ratio $m = 3$ is used, leading to an eye-opening improvement factor of 6. Fig. 12 shows the simulated output eye diagrams of the high-speed latches based on various circuit topologies for comparison. It is noted that the capacitive-splitting CML latch with the NE topology exhibits the best quality in the output characteristics, making it very attractive for high-speed applications.

Fig. 13 illustrates the schematic of the two-stage differential amplifiers, which provide the required buffering for the deserialized output data. To prevent the degradation in the bandwidth of the latches for high-speed operations, the first amplifier stage is designed to minimize the capacitive loading of the MS-FFs, while maintaining moderate signal amplification. On the other hand, the second amplifier stage is employed to steer a large output current for sufficient voltage swing across the external load of 50 Ω .

IV. EXPERIMENTAL RESULTS

The proposed DEMUX is implemented in a standard 1P6M 0.18- μ m CMOS process. Fig. 14 shows the microphotograph of the fabricated circuit with a chip area of 0.92×0.82 mm² including the pads. In order to evaluate the high-speed characteristics of the proposed technique, the fabricated circuit was tested by on-wafer probing. Fig. 15 shows the measurement setup, where the differential input data are generated by a pattern generator and a 4:1 multiplexer, and a single-ended clock at half of the data rate is provided by a synchronized signal generator with an output phase shifter. The single-ended voltage swings for the input data and the clock signal are 0.6 and 1 V_{pp}, respectively.

With a 2-V supply voltage, the DEMUX consumes a dc power of 150 mW including the output buffers. The fabricated circuit was first tested in the re-time mode to evaluate the highest operating speed of the MS-FFs with the capacitive-splitting CML latches. Fig. 16 shows the re-timed single-ended eye diagram

at the MS-FF output for a 13-Gb/s data rate and a 13-GHz clock, exhibiting a voltage swing of 250 mV_{pp}. The measured peak-to-peak and rms jitter are 27.14 and 4.14 ps, respectively. With a $2^{23} - 1$ PRBS at a data rate of 20 Gb/s and a 10-GHz half-rate clock, the measured output single-ended eye diagram of the DEMUX is shown in Fig. 17. The obtained eye opening is 150 mV, while the measured peak-to-peak and rms jitter are 21.2 and 3.6 ps, respectively. Note that, due to the limitations of the testing instruments, the measurement results are based on a single-ended clock signal. According to the simulation results, a higher data rate at 25 Gb/s can be achieved with differential clock signal provided. A comparison with the state-of-the-art results from previously published studies is tabulated in Table I.

V. CONCLUSION

In this paper, two different types of capacitive-splitting architectures, which are proposed to enhance the bandwidth and the operation speed of CML latches, have been analyzed and discussed. Based on the proposed circuit technique, a high-speed 1:2 DEMUX circuit is presented in a 0.18- μ m CMOS process. With a $2^{23} - 1$ PRBS input, the fabricated circuit operates at a maximum data rate of 20 Gb/s, exhibiting a significant performance improvement compared with conventional topology with static CML latches.

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