Design of Ultra-Low-Voltage RF Frontends With Complementary Current-Reused Architectures

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Abstract—In this paper, ultra-low-voltage circuit techniques are presented for CMOS RF frontends. By employing a complementary current-reused architecture, the RF building blocks including a low-noise amplifier (LNA) and a single-balanced down-conversion mixer can operate at a reduced supply voltage with microwatt power consumption while maintaining reasonable circuit performance at multigigahertz frequencies. Based on the MOSFET model in moderate and weak inversion, theoretical analysis and design considerations of the proposed circuit techniques are described in detail. Using a standard 0.18- μm CMOS process, prototype frontend circuits are implemented at the 5-GHz frequency band for demonstration. From the measurement results, the fully integrated LNA exhibits a gain of 9.2 dB and a noise figure of 4.5 dB at 5 GHz, while the mixer has a conversion gain of 3.2 dB and an IIP_3 of -8 dBm. Operated at a supply voltage of 0.6 V, the power consumptions of the LNA and the mixer are 900 and 792 μW , respectively.

Index Terms—CMOS RF frontends, complementary current-reused topology, down-conversion mixers, low-noise amplifiers (LNAs), moderate inversion, ultra-low power, ultra-low voltage.

I. INTRODUCTION

AS THE feature size of MOSFETs continues to shrink, a proportional downscaling in the supply voltage is mandatory to maintain gate-oxide reliability [1]. However, in consideration of the subthreshold leakage and the noise margin required by the digital integrated circuits, the scaling rate of the threshold voltage is relatively slow compared with that of the supply voltage. Consequently, the overdrive voltage of the transistors progressively decreases as the technology advances. It has become an inevitable trend to operate the MOS devices in moderate or weak inversion for certain mixed-signal and RF integrated circuits, motivating the development of low-voltage design techniques exclusively for deep-submicrometer CMOS technologies [2]–[6].

In an RF receiver frontend, the low-noise amplifier (LNA) and the down-conversion mixer are considered the most important building blocks. Typically, these circuits suffer from significant degradation in the RF properties, especially for gain, noise figure, and linearity, as the transistors operate in weak inversion. To overcome the limitations on the supply voltage and the transistor overdrive, a complementary current-reused topology has been proposed for the RF frontend circuits [7], [8]. Using a stan-

dard 0.18- μm CMOS process, an ultra-low-voltage LNA and mixer suitable for operations with microwatt power consumption are realized at the 5-GHz frequency band. The behavior of the MOSFETs biased at a reduced overdrive voltage and its impact on the circuit performance of RF frontends are also investigated. Though the fabricated circuits are not targeted at a specific wireless standard, the developed techniques and design guidelines can be easily applied for various short-range wireless applications such as ZigBee, Bluetooth, wideband personal area network (WPAN), and wireless sensor networks.

This paper is organized as follows. In Section II, MOSFETs biased at different inversion levels are reviewed, and a transistor model suitable for moderate and weak inversion is introduced. The proposed circuit topologies of the LNA and the down-conversion mixer are described in Sections III and IV, respectively. Section V presents the design and experimental results of the 5-GHz RF frontends. Finally, a conclusion is provided in Section VI.

II. MOSFETs AT VARIOUS INVERSION LEVELS

For the design of the RF frontend circuits operating at ultra-low supply voltage and power consumption, the behavior of the MOSFETs with a reduced overdrive voltage is first investigated and modeled. In conventional circuit implementations, the transistors are normally biased in their saturation regions to maximize the transconductance and output resistance. Depending on the gate-to-source voltage (V_{GS}), the operation of the MOSFETs is typically classified into three modes: weak, moderate, and strong inversion. Weak inversion indicates that the value of V_{GS} is slightly higher than the threshold voltage V_{th} . With the insufficient number of carriers in the induced channel, the drain current (I_D) is dominated by the diffusion component instead of the drift one. Consequently, the device exhibits exponential I - V characteristics. As V_{GS} increases, the drift current becomes more significant. It is often referred to as moderate inversion when the carrier drift reaches a level comparable to the diffusion current. Finally, the drain current is dominated by the carrier drift when a high gate voltage is applied, leading to strong inversion operation with a square-law I - V relationship.

In order to perform theoretical analysis for circuit designs, it is desirable to have a more quantitative scale of the inversion level for the MOSFETs. A useful index “inversion coefficient” is defined in [9] and [10] by a normalized drain current, which can be expressed as

$$IC = \frac{I_D}{I_0 \left(\frac{W}{L} \right)}. \quad (1)$$

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Fig. 1. Simulated saturated drain current and the associated inversion coefficient of an n -channel MOSFET with a fixed V_{DS} .

Note that I_D is the saturation drain current, W and L are the effective channel width and length, respectively, and I_0 is the technology current, which is process dependent, and is defined as

$$I_0 = 2n\mu_0 C_{ox} V_T^2 \quad (2)$$

where n is the weak-inversion slope factor with a typical value from 1 to 2, μ_0 is the low-field mobility, C_{ox} is the gate-oxide capacitance per unit area, and V_T is the thermal voltage. Conventionally, the device is considered in weak inversion for $IC < 0.1$ and in strong inversion for $IC > 10$. For an IC value ranging from 0.1 to 10, the MOS transistor is operating in moderate inversion. To have a better understanding on the bias condition of the transistors, simulated I_D versus V_{GS} for a 0.18- μm nMOS device under a fixed drain-to-source voltage (V_{DS}) is illustrated in Fig. 1, where the values of IC is obtained from (1) with a technology current of 0.7 μA . According to the definition, it is observed that the transistor operate in weak inversion for $V_{GS} < 0.4$ V and in strong inversion for $V_{GS} > 0.7$ V. With V_{GS} between 0.4 and 0.7 V, the transistor is biased in moderate inversion.

With various levels of inversion, the I - V characteristics of the MOSFETs are strongly influenced by the bias condition. Typically, distinct expressions of the drain current are required for weak, moderate, and strong inversion to characterize the transistor behavior. For simplicity, a semiempirical expression of the saturation current evolved in [11] and [12] is employed for the analysis and design of the RF frontend circuits in this paper. The saturation current of a MOSFET is given by

$$I_D = I_{D0} \left\{ \ln \left[1 + \exp \left(\frac{V_{GS} - V_{th}}{2nV_T} \right) \right] \right\}^2 \quad (3)$$

with

$$I_{D0} = 2\mu_0 C_{ox} n V_T^2 \left(\frac{W}{L} \right). \quad (4)$$

For a MOS transistor operating in strong inversion, the drain current in (3) can be approximated by

$$I_D = \mu_0 C_{ox} \left(\frac{W}{L} \right) \cdot \frac{(V_{GS} - V_{th})^2}{2n}. \quad (5)$$

Fig. 2. Simulated and the calculated drain currents of a 0.18- μm n -channel MOSFET operating in the saturation region with a fixed V_{DS} .

Note that (5) has the well-known form of the square-law I - V characteristics.

For short-channel devices, the nonideal effects such as velocity saturation, series drain-source resistance, and mobility degradation should also be taken into account for the device modeling. As a result, a modified current expression of (3) is given by [13]

$$I_D = \frac{\mu_0 C_{ox} W}{2nL} \cdot \frac{X^2}{1 + \rho X} \cdot (1 + \lambda V_{DS}) \quad (6)$$

where

$$X = 2nV_T \ln \left[1 + \exp \left(\frac{V_{GS} - V_{th}}{2nV_T} \right) \right] \quad (7)$$

$$\rho = \theta + \frac{\mu_0}{2nv_{sat}L}. \quad (8)$$

Here, the parameters θ and v_{sat} are the mobility reduction coefficient and the saturation velocity, respectively. From (7), the transconductance (g_m) and the zero-bias drain conductance (g_{d0}) of the device can be derived and are given by

$$g_m = \frac{\mu_0 C_{ox} W}{2nL} \cdot \left(\frac{X}{1 + \rho X} + \frac{X}{(1 + \rho X)^2} \right) \cdot \left\{ 1 - \left[\exp \left(\frac{X}{2nV_T} \right) \right]^{-1} \right\} \cdot (1 + \lambda V_{DS}) \quad (9)$$

$$g_{d0} = \frac{\mu_0 C_{ox} \lambda W}{2nL} \cdot \frac{X^2}{1 + \rho X}. \quad (10)$$

In order to verify the device model, the simulated saturation current as a function of V_{GS} along with the values obtained from (6) are plotted in Fig. 2. It is observed that (6) predicts the drain current of the MOSFET operating from weak to strong inversion with sufficient accuracy. Therefore, the derivations in (6)–(10) are employed for the analysis of the RF frontend circuits below.

III. PROPOSED LNA

A. Circuit Topology

To operate the LNA at reduced supply voltage and power consumption while providing sufficient gain at multigigahertz frequencies, a complementary amplifier with a current-reused

Fig. 3. Evolution of the proposed LNA. (a) Conventional cascode topology. (b) CMOS amplifier topology. (c) Complementary current-reused topology with two cascaded gain stages. (d) Complementary current-reused topology with three cascaded gain stages.

circuit topology is presented. The evolution of the proposed low-voltage technique is illustrated in Fig. 3. In conventional circuit implementations, a cascode amplifier [14], as shown in Fig. 3(a), is widely used for the LNA designs. With the current-reused feature in the cascode topology, desirable LNA gain is achieved with relatively low current consumption. However, it is not suitable for low-voltage operations due to the stack of nMOS transistors. In order to alleviate the limitations imposed on the supply voltage, an LNA topology, as shown in Fig. 3(b), has been proposed [15]. Due to the use of the CMOS amplifier stages, the required supply voltage is reduced by one transistor overdrive compared with that of the cascode amplifiers. Unfortunately, the gain of the CMOS LNAs is inherently low, especially for low-power operations. For an enhanced gain in ultra-low-power and ultra-low-voltage designs, a complementary current-reused LNA topology with cascaded amplifier stages is proposed, as shown in Fig. 3(c). Note that, under similar bias conditions, the amplifier gain can be further enhanced by increasing the number of cascaded stages in the proposed LNA architecture, as illustrated in Fig. 3(d). However, in practical circuit implementations, the parasitics introduced by the additional gain stages may result in performance degradation. Therefore, an LNA with three cascaded gain stages is employed in this study.

The complete circuit schematic of the LNA is shown in Fig. 4, where common-source MOS transistors M_1 , M_2 , and M_3 represent the first, second, and third gain stages, respectively. By connecting the drain inductance of each transistor together with an ac ground provided by the bypass capacitor C_4 , the complementary current-reused topology is established. As for the dc bias, the gate of M_1 is connected to V_{DD} , while those of M_2 and M_3 are tied to the ground through resistors. In order to obtain simultaneous power and noise matching for the input stage, the inductive source degeneration with L_1 and L_2 is adopted. On the other hand, the output matching is provided by L_7 and C_3 . The LC networks $L_3 - C_1$ and $L_5 - C_2$ between the gain stages are used for inter-stage matching.

Fig. 4. Complete circuit schematic of the proposed LNA suitable for ultra-low-voltage and ultra-low-power applications.

B. Theoretical Analysis

In order to evaluate the circuit performance and to provide useful design guidelines of the proposed LNA for low-voltage and low-power operations, theoretical analysis is performed with respect to the circuit specifications using the MOSFET model, as presented in Section II.

1) *Small-Signal Characteristics*: As the first active building block in an RF receiver, the LNA is required to provide sufficient gain such that the noise contributed from the following stages can be effectively suppressed. Note that the proposed circuit topology is basically a three-stage amplifier, as illustrated in Fig. 5. To achieve a maximum available gain of the LNA, the effective transconductance (G_m) of the cascaded stages should be optimized, while power matching is required in between the

Fig. 5. Circuit schematic of an equivalent three-stage cascaded amplifier with the input, output, and inter-stage matching networks.

stages. Assuming that the losses from the matching network are negligible, the conjugate matching conditions are given by [16]

$$Z_S = Z_{IN,1}^* \quad (11)$$

$$Z_{OUT,1} = Z_{IN,2}^* \quad (12)$$

$$Z_{OUT,2} = Z_{IN,3}^* \quad (13)$$

$$Z_{OUT,3} = Z_L^* \quad (14)$$

In addition to the amplifier gain, the noise figure is also an important design consideration for the impedance matching of the LNA circuits. The matching conditions for minimum noise figures of the cascaded gain stages are given by

$$Z_S = Z_{opt,1} \quad (15)$$

$$Z_{OUT,1} = Z_{opt,2} \quad (16)$$

$$Z_{OUT,2} = Z_{opt,3} \quad (17)$$

where $Z_{opt,1}$, $Z_{opt,2}$, and $Z_{opt,3}$ are the optimum noise source impedances for the first, second, and third stages, respectively. In typical LNA designs, it is difficult to meet (11)–(17) at the same time. However, due to the use of the source degeneration in the cascaded gain stages, simultaneous power and noise matching can be achieved [17], leading to optimum performance of the LNA.

With the matching conditions specified in (11)–(17), the effective transconductance of the gain stages can be derived as

$$G_{m1} = \frac{g_{m1}}{2\omega_0 C_{gs1} R_S} \quad (18)$$

$$G_{m2} = \frac{g_{m2}}{2\omega_0 C_{gs2} \text{Re}(Z_{IN,2})} \quad (19)$$

$$G_{m3} = \frac{g_{m3}}{2\omega_0 C_{gs3} \text{Re}(Z_{IN,3})} \quad (20)$$

where ω_0 is the operating frequency, R_S is the source impedance, and g_m and C_{gs} represent the transconductance

and gate-to-source capacitance of the MOSFETs, respectively. Generally, the capacitance C_{gs} is given by

$$C_{gs} \approx mWLC_{ox} \quad (21)$$

where m is a constant with a value of $2/3$ for long-channel devices. By combining (9) and (21), the cutoff frequency, which is defined as the ratio of g_m and C_{gs} , is expressed as

$$\begin{aligned} \omega_T &\equiv \frac{g_m}{C_{gs}} \\ &\approx \frac{\mu_0}{2mnL^2} \cdot \left[\frac{X}{1 + \rho X} + \frac{X}{(1 + \rho X)^2} \right] \\ &\quad \cdot \left\{ 1 - \left[\exp\left(\frac{X}{2nV_T}\right) \right]^{-1} \right\} \cdot (1 + \lambda V_{DS}). \end{aligned} \quad (22)$$

From (18)–(20), it is clear that the effective transconductance of the gain stages is strongly influenced by the transistor overdrive voltage. Therefore, three cascaded stages are employed in the proposed LNA topology to boost the amplifier gain for ultra-low-voltage operations. Note that, from (19)–(20), transconductances of the second and third stages can be effectively enhanced by reducing the real part of $Z_{IN,2}$ and $Z_{IN,3}$. However, it usually requires transistors with enormous aspect ratios for noise matching, leading to performance degradation, especially at higher frequencies, due to the excessive parasitics from the MOSFETs.

Another important specification of the LNA circuits is the impedance matching at the input. The small-signal equivalent circuit of the first gain stage is illustrated in Fig. 6, where Z_{L1} is the load impedance. Note that, due to the existence of C_{gd1} , the input stage is treated as a bilateral two-port network and the input impedance is influenced by Z_{L1} . Assuming that the overlap capacitance C_{gd1} is relatively small, which is generally

Fig. 6. Small-signal equivalent circuit of the input stage.

the case in practical designs, a simplified expression of the input impedance is given by

$$Z_{IN} \approx s(L_1 + L_2) + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_2}{C_{gs1}}. \quad (23)$$

From (23), the input impedance matching to a 50-Ω system can be achieved by

$$\frac{g_{m1}L_2}{C_{gs1}} = 50 \quad (24)$$

$$\omega_0 = \frac{1}{\sqrt{(L_1 + L_2)C_{gs1}}}. \quad (25)$$

2) Noise Figure: In a typical RF system, the sensitivity of the receiver is determined by the noise figure of the LNA. Due to the use of the source degeneration in the amplifier stages, noise and power matching can be simultaneously achieved. Provided that the gain is sufficiently larger, the noise figure of a cascaded LNA is dominated by the input stage. To have a better understanding on the noise matching, the equivalent circuit of the input stage is depicted in Fig. 7, where v_{ns} and Z_{ns} indicate the Thevenin's equivalent circuit seen from the MOS transistor to the source terminal, and $\overline{i_{ng}^2}$ and $\overline{i_{nd}^2}$ represent the mean-square values of the gate-induced and channel noise currents, respectively. The expressions of the noise currents are given by

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \quad (26)$$

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \Delta f \quad (27)$$

where δ and γ have typical values of 4/3 and 2/3, respectively. Note that g_g is given by

$$g_g = \frac{\omega^2 C_{gs1}^2}{5g_{d0}} \quad (28)$$

where g_{d0} is the zero-bias drain conductance. Assuming that the effects of C_{gd1} and r_{o1} are negligible, the two-port noise parameters of the equivalent circuit in Fig. 7 can be derived. The noise resistance R_n , the optimum source impedance $Z_{opt,1}$, and the minimum noise factor F_{min} are expressed as [17], [18] follows:

$$R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_{m1}} \quad (29)$$

Fig. 7. Small-signal equivalent circuit of the LNA input stage with noise current sources.

$$Z_{opt,1} \approx \frac{\sqrt{\frac{\alpha^2 \delta}{5\gamma}} (1 - |c|^2)}{\omega_0 C_{gs1} \left[\frac{\alpha^2 \delta}{5\gamma} (1 - |c|^2) + \left(1 + \sqrt{\frac{\alpha^2 \delta |c|^2}{5\gamma}} \right)^2 \right]} \quad (30)$$

$$F_{min} = 1 + \frac{2\omega_0}{\sqrt{5}\omega_T} \sqrt{\gamma \delta (1 - |c|^2)} \quad (31)$$

where $\alpha = g_m/g_{d0}$ and $|c|$ is a correlation coefficient with a predicted value of 0.395 [14]. Note that η can be expressed as

$$\eta = \frac{1 + \sqrt{\frac{a^2 \delta |c|^2}{5\gamma}}}{\left[\frac{a^2 \delta}{5\gamma} (1 - |c|^2) + \left(1 + \sqrt{\frac{a^2 \delta |c|^2}{5\gamma}} \right)^2 \right]} \quad (32)$$

and has a value close to unity. From the equivalent circuit in Fig. 7, the input impedance $Z_{IN,1}$ at the gate of M_1 is approximated by

$$Z_{IN,1} \approx sL_2 + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_2}{C_{gs1}}. \quad (33)$$

According to (30) and (33), the simultaneous power and noise matching can be achieved if $Z_{opt,1}$ is the complex conjugate of $Z_{IN,1}$, resulting in

$$\frac{g_{m1}L_2}{C_{gs1}} = \frac{\sqrt{\frac{\alpha^2 \delta}{5\gamma}} (1 - |c|^2)}{\omega_0 C_{gs1} \left[\frac{\alpha^2 \delta}{5\gamma} (1 - |c|^2) + \left(1 + \sqrt{\frac{\alpha^2 \delta |c|^2}{5\gamma}} \right)^2 \right]}. \quad (34)$$

By properly choosing the device parameters to satisfy (34), the input stage of the LNA exhibits a noise factor of F_{min} while maintaining a maximum power gain and a low input return loss at the operating frequency ω_0 .

To further investigate the influence of the bias conditions on the minimum noise factor F_{min} , the simulated values along with the calculated ones from (22) and (31) are demonstrated in Fig. 8, which provides useful guidelines for the design of

Fig. 8. Simulated and calculated minimum noise factor of a 0.18- μm n -channel MOSFET with a fixed V_{DS} .

the LNAs at various bias conditions. It is obvious that $F_{\min}$ increases as the bias voltage V_{GS} decreases. For ultra-low-voltage LNAs with the MOSFETs operated in moderate inversion, the $F_{\min}$ obtained from the device model in (22) can be treated as the worst case estimation in practical circuit implementations.

3) *Linearity*: With the ultra-low supply voltage and power consumption in the LNA design, the small-signal approximation only holds at a reduced input power. As the signal level increases, nonlinear characteristics such as gain compression and intermodulation distortion become significant. Therefore, analysis on the linearity of the proposed LNA is essential for practical applications. Due to the similarity in the circuit topology, the proposed LNA is considered as a three-stage cascaded amplifier to simplify the analysis. By neglecting the dc and higher order harmonic terms in the transfer function, the input third-order intercept point (IIP₃) of the LNA is given by [14]

$$\frac{1}{\text{IIP}_3} \approx \frac{1}{\text{IIP}_{3,1}} + \frac{a_1^2}{\text{IIP}_{3,2}} + \frac{a_1^2 b_1^2}{\text{IIP}_{3,3}} \quad (35)$$

where a_1 and b_1 are the linear gains of the first and the second stage, respectively. Assuming that a_1 and b_1 are greater than unity, the input intermodulation distortion of the third stage dominates. Therefore, analysis on the linearity of the third stage is employed to evaluate the overall LNA performance.

To investigate the linearity of the amplifier stage, the drain current of M_3 is expressed by a third-order power series as

$$i_{d3} \approx c_1 v_{sg3} + c_2 v_{sg3}^2 + c_3 v_{sg3}^3. \quad (36)$$

Since the third-order derivative of the drain current with respect to gate voltage is the major contribution to the distortion, it is required to derive the coefficient c_3 . Based on the transistor model in (6), c_3 is given by [13]

$$c_3 = -\frac{\mu_0 C_{ox} W}{2nL} \cdot \frac{\kappa(1 + \lambda V_{SD})}{24n^2 V_T^2 (1 + \kappa)^3 (1 + \rho Y)^4} \cdot \left[24n^2 V_T^2 \kappa^2 \rho - 12n V_T \kappa (1 + \rho Y) + Y(\kappa - 1)(2 + \rho Y)(1 + \rho Y)^2 \right] \quad (37)$$

Fig. 9. Calculated IIP₃ of the gain stage versus gate bias voltage V_{SG} for various values of $R_{IN,3}$.

where

$$\kappa = \exp\left(\frac{V_{SG3} - V_{th}}{2nV_T}\right) \quad (38)$$

$$Y = 2nV_T \ln \left[1 + \exp\left(\frac{V_{SG3} - V_{th}}{2nV_T}\right) \right]. \quad (39)$$

As indicated in [14], IIP₃ can be approximated by

$$\text{IIP}_3 \approx \frac{2}{3R_{IN,3}} \left(\frac{c_1}{c_3} \right) \quad (40)$$

where $R_{IN,3}$ represents the input resistance of M_3 . Since c_1 is actually the transconductance (g_m) of the MOSFET, IIP₃ can be derived by substituting (9) and (37) into (40) as [13]

$$\text{IIP}_3 \approx \frac{32n^2 V_T^2 (1 + \kappa)^2 Y (1 + \rho Y)}{R_{IN,3}} \cdot \left[24n^2 V_T^2 \kappa^2 \rho - 12n V_T \kappa (1 + \rho Y)^3 + Y(\kappa - 1)(2 + \rho Y)(1 + \rho Y)^2 \right]^{-1}. \quad (41)$$

Based on (41), the calculated IIP₃ versus V_{SG} is depicted in Fig. 9. It is clear that the IIP₃ of the MOSFETs in the amplifiers generally increases with the gate bias voltage. However, with the source degeneration in the cascaded gain stages, the coefficient c_1 in (40) is no longer the transconductance g_{m3} , but the effective transconductance of the third stage G_{m3} , as specified in (20). Thus, in the proposed LNA topology, the gain of the third stage can be traded for enhanced amplifier linearity, especially when low-voltage operations are required.

4) *Stability Consideration*: The stability is another important issue in LNA designs, and can be inspected by the reflection coefficients at the matching networks and terminations. For a general two-port network, in order not to initiate the undesirable oscillation, the necessary and sufficient conditions for the circuit stability are given by [16]

$$|\Gamma_s| < 1 \quad (42)$$

$$|\Gamma_l| < 1 \quad (43)$$

$$|\Gamma_i| = \left| S_{11} + \frac{S_{12} S_{21} \Gamma_l}{1 - S_{22} \Gamma_l} \right| < 1 \quad (44)$$

$$|\Gamma_o| = \left| S_{22} + \frac{S_{12} S_{21} \Gamma_s}{1 - S_{11} \Gamma_s} \right| < 1 \quad (45)$$

Fig. 10. Evolution of the proposed down-conversion mixer. (a) Conventional Gilbert-cell mixer. (b) Folded cascode topology. (c) Complementary current-reused topology. (d) Complementary current-reused topology with the current-bleeding technique.

where Γ_s , Γ_1 , Γ_i , and Γ_o represent the source, load, input, and output reflection coefficients, respectively. With proper rearrangement, (42)–(45) result in the following two conditions:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (46)$$

$$|\Delta| < 1 \quad (47)$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \quad (48)$$

Note that (46) and (47) are derived for a single-stage amplifier. For multistage ones, the conditions for unconditional stability should be applied to each one of the gain stages. That is, once each gain stage in the cascaded topology satisfies (46) and (47), the stability of the amplifier is assured. In this particular design, the simplified circuit model in Fig. 5 is adopted to examine the circuit stability. Due to the use of the source degeneration, which is considered a negative feedback at the frequencies of interest, for each one of the gain stages, the proposed amplifier satisfies the unconditionally stable conditions at various process corners.

5) *Bias Conditions*: Due to the use of the complementary stages for the LNA design, the voltage at the drain of the MOSFETs (V_P), as shown in Fig. 4, is considered a quasi-stable dc point under normal bias conditions. Typically, a common-mode feedback (CMFB) is required to provide a stable dc bias at the output. In the proposed topology, the transistors are inevitably operated in moderate or weak inversion due to the reduce supply voltage. The drain currents of the MOSFETs are saturated even with a V_{DS} smaller than $V_{GS} - V_{th}$. Thus, by properly selecting the aspect ratios of the transistors, the voltage V_P can endure process and supply voltage variations to provide a relatively stable bias for the amplifier even without the CMFB. According to the circuit simulations, a voltage shift less than 50 mV is observed at V_P with a $\pm 5\%$ variation in the supply voltage for various corner analyses.

IV. PROPOSED DOWN-CONVERSION MIXER

A. Proposed Topology

Fig. 10(a) shows a simplified circuit topology of a Gilbert cell, which is widely used as the down-conversion mixer in RF frontends. The transistor M_1 acts as the transconductance stage to convert the RF voltage into a current signal, while M_2 and M_3 form the communicating stage for frequency translation. With the series-gated topology, the Gilbert cells are not suitable for low-voltage applications. In order to reduce the required supply voltage, a folded cascode mixer [19] is proposed, as shown in Fig. 10(b). Since the dc current reuse between the transconductance and commuting stages no longer exists, the power consumption may increase even with a reduced supply voltage. For low-power and low-voltage applications, the proposed complementary current-reused technique is adopted for the down-conversion mixer as well. A conceptual illustration of the proposed mixer topology is shown in Fig. 10(c), where an nMOS transconductance stage and a pMOS commuting stage are stacked between the V_{DD} and the ground. To enhance the gain of the down-conversion mixer, the current-bleeding technique [20] can also be incorporated into the proposed topology, as shown in Fig. 10(d).

The complete circuit schematic of the down-conversion mixer is illustrated in Fig. 11. The RF current generated by the transconductance of M_1 is directed to the source of the switching pair through the bypass capacitor C_1 , while the frequency translation of the single-balanced mixer is provided by the commuting stage $M_2 - M_3$. In the mixer design, the load resistance R_L is selected to maximize the conversion gain. For low-voltage operations, the current-bleeding technique is adopted by using the resistor R_1 as the current source. As part of the bias current flows through R_1 , excess voltage drop across R_L can be prevented even with large load resistance. As a result, the mixer can operate at a reduced supply voltage while providing sufficient conversion gain for frequency translation. Note that source degeneration with on-chip inductors L_1 and L_2 is also employed for the transconductance stage to provide

Fig. 11. Complete circuit schematic of the proposed down-conversion mixer suitable for ultra-low-voltage and ultra-low-power applications.

Fig. 12. Equivalent circuit model of the proposed mixer for the derivation of the down-conversion gain.

signal amplification and impedance matching at RF frequencies. To have a better understanding of the proposed mixer circuit, detailed analysis with respect to the most important circuit specifications is presented as follows.

B. Theoretical Analysis

1) *Conversion Gain*: The conversion gain of the mixer is evaluated by the equivalent circuit, as shown in Fig. 12. Assuming that the input impedance is matched to 50Ω and the local oscillator (LO) signals are square waves, the conversion gain is approximately by

$$CG \approx \frac{g_{m1}}{50\pi\omega_{RF}C_{gs1}} \cdot \frac{g_{m2}\omega_{RF}L_3}{\sqrt{1 + g_{m2}^2\omega_{RF}^2L_3^2}} \cdot R_L \quad (49)$$

where ω_{RF} is the RF frequency, and g_{m1} and g_{m2} are the transconductances of M_1 and M_2 , respectively. The expression in (49) can be further simplified as

$$CG \approx \frac{g_{m1}R_L}{50\pi\omega_{RF}C_{gs1}}, \quad \text{for } g_{m2} \gg \frac{1}{\omega_{RF}L_3} \quad (50)$$

$$CG \approx \frac{g_{m1}g_{m2}L_3R_L}{50\pi C_{gs1}}, \quad \text{for } g_{m2} \ll \frac{1}{\omega_{RF}L_3}. \quad (51)$$

Fig. 13. Simulated normalized conversion gain (CG) and noise figure (NF) of the proposed mixer as functions of the current bleeding ratio.

According to (50) and (51), the conversion gain is independent of the commuting stage when g_{m2} is sufficiently large, and decreases with g_{m2} as the transconductance of the commuting stage becomes too small.

Due to the use of the current-bleeding technique, large load resistance R_L can be employed to enhance the conversion gain. However, as more current flows through R_1 , the transconductance of the commuting stage diminishes, leading to a degraded conversion gain, as predicted in (51). The optimum conversion gain can be achieved by taking the effects of both R_L and g_{m2} into consideration. With the definition of the current-bleeding ratio (χ) as the dc current through R_1 divided by the total bias current, the simulated conversion gain versus χ is presented in Fig. 13. It is observed that the down-conversion mixer exhibits a maximum conversion gain with a current-bleeding ratio of 90% in this particular design. In addition to the conversion gain, the simulated noise figure is also depicted in Fig. 13, indicating an increase in the noise figure as χ approaches to unity. Therefore, a tradeoff is involved between the conversion gain and the noise figure for circuit implementations. Note that the derivation in (49) is based on the small-signal equivalent circuits of the mixer. Hence, the linearity issue is not taken into account. It is generally true that the current-bleeding technique enhances the down-conversion gain at the cost of the circuit linearity. In order to alleviate such limitations, the transconductance stage of the proposed mixer is biased in the vicinity of the “sweet spot” to boost IIP_3 . More detailed derivation and analysis will be presented in Section IV-B.2.

2) *Linearity*: In a receiver frontend, the linearity and dynamic range are strongly influenced by the down-conversion mixer. To simplify the analysis, the linearity of the mixer is evaluated by the characteristics of the transconductance stage with the assumption that the commuting stage acts as ideal switches. For a saturated MOSFET, the simulated IIP_3 along with the values of c_1 and c_3 , which are defined in (36), are illustrated in Fig. 14. As V_{GS} increases, the transistor operates from weak to strong inversion, leading to an increase in the value of c_1 . On the other hand, the value of c_3 turns from positive to negative with a zero-crossing point at V_{GS} slightly higher than V_{th} . It is obvious that the IIP_3 of the mixer increases with V_{GS} when the transistor is operating in strong inversion. For the transistor

Fig. 14. (a) Simulated IIP_3 and (b) the associated coefficients c_1 and c_3 of the n -channel MOSFET at various gate bias voltages.

Fig. 15. Simulated ΔIIP_3 of the proposed mixer with various values of L_2 for inductive source degeneration.

in the moderate inversion, interestingly, a significant peaking in the magnitude of IIP_3 is observed at the zero-crossing point of c_3 , which is typically referring to as the “sweet spot” [13]. Therefore, by properly biasing the transconductance stage of the mixer in the vicinity of the sweet spot, an enhanced IIP_3 can be achieved even with a reduced supply voltage. In the proposed mixer circuit, source degeneration is employed for input matching at the RF frequencies. Fig. 15 shows the simulated deviation in the IIP_3 of the mixer biased at the sweet spot with various values of the source inductance L_2 . Based on the simu-

Fig. 16. Simplified illustration of the LO leakage paths to the RF port in the proposed mixer.

Fig. 17. Design flow of the proposed complementary current-reused LNA.

lation results, the IIP_3 peaking at the sweet spot degrades due to the use of the source inductance. Therefore, special care has to be taken in selecting the values of the source degeneration for optimum circuit performance in terms of the input matching, conversion gain, and linearity.

3) *Isolation*: To reduce the overall power consumption of the RF frontends, low-or zero-IF architectures appear to be particularly well suited for the frequency down-conversion. Consequently, the isolation between the LO and RF ports becomes critically important. Fig. 16 shows a simplified illustration of the LO leakage paths to the RF port in the proposed mixer. In addition to the possible coupling through the gate-to-source capacitance C_{gs} of the commuting stage, which is similar to the case

TABLE I
CIRCUIT PARAMETERS OF THE LNA

Devices	Design Values
M_1	100 μm / 0.18 μm
M_2	175 μm / 0.18 μm
M_3	175 μm / 0.18 μm
L_1	3.8 nH
L_2, L_4, L_6	0.6 nH
L_3, L_5, L_7	1.6 nH
C_1, C_2	1.8 pF
C_3	0.5 pF

Fig. 18. Microphotograph of the fabricated LNA.

in conventional Gilbert-cell mixers, the signal path provided by the parasitic capacitance C_{gd} of the switching pair should also be taken into account. Fortunately, with the current-bleeding technique, large load resistance R_L is allowed for the mixer design. The LO leakage to the RF port through C_{gd} is generally insignificant and can be neglected. Due to the differential operation in terms of the LO signals, the fundamental coupling is theoretically cancelled out at the common-mode nodes, and the LO-to-RF isolation is solely resulted from the mismatch between the MOS devices and the load resistances. With careful selection of the design parameters accompanied by a symmetric layout, port isolation better than 30 dB can be achieved for applications at multigigahertz frequencies.

4) *DC Stability*: With the complementary current-reused stages, dc stability should be carefully examined in the mixer design. As shown in Fig. 11, the voltage at the drain of the MOSFETs is considered a quasi-stable dc point and is generally susceptible to variations in the fabrication process and the supply voltage. Fortunately, with the current bleeding introduced by R_1 , only a small portion of the bias current flows through the pMOS switching pair. The drain voltage of M_1 is thus defined by R_1 , leading to good bias stability. From the simulation results, the drain voltage (V_Q) has a deviation less

Fig. 19. Measured (solid lines) and simulated (dotted lines) small-signal parameters of the LNA.

Fig. 20. Two-tone harmonic measurement of the 5-GHz LNA with an input frequency spacing of 20 MHz.

than 70 mV with respect to the supply voltage variation up to $\pm 5\%$ for various corner conditions in this particular design.

V. CIRCUIT DESIGN AND EXPERIMENTAL RESULTS

In order to demonstrate the feasibility of ultra-low-voltage RF frontends with the proposed circuit technique, an LNA and a down-conversion mixer are designed to operate at a supply voltage of 0.6 V for 5-GHz applications. The circuits are implemented in a standard 0.18- μm CMOS technology provided by a commercial foundry. The threshold voltages of

TABLE II
PERFORMANCE COMPARISON OF LOW-VOLTAGE AND LOW-POWER LNAS

	Unit	This Work	[21]		[22]		[23]
Technology	—	0.18- μm CMOS	0.35- μm SOI		0.18- μm CMOS		90-nm CMOS
Frequency	GHz	5.0	1.6		5.8		5.5
Supply Voltage	V	0.6	1.5	0.6	1.0	0.7	0.6
DC Power	mW	0.9	7.5	1.2	22.2	12.5	1.0
Power Gain	dB	9.2	10.8	6.4	13.2	7.0	9.2
Noise Figure	dB	4.5	4.2	4.8	2.5	2.9	3.6
$ S_{11} $	dB	-12	—	—	-5	-7	-10
$ S_{22} $	dB	-21	—	—	-10	-12	-14
$P_{\text{in-1dB}}$	dBm	-27	4	—	-14	-9	-16
IIP ₃	dBm	-16	—	—	—	—	-7
Gain/ P_{dc}	dB/mW	10.2	1.4	5.3	0.6	0.6	9.2

the nMOS and pMOS transistors are approximately 0.5 V. As for the on-chip passive components, a top AlCu metallization layer of 2- μm thickness is available for the inductive elements, while the metal–insulator–metal (MIM) capacitors with oxide intermetal dielectric are also provided. The RF performance of the LNA and the mixer is characterized by on-wafer probing.

A. LNA

With the circuit schematic, as shown in Fig. 4, the design procedure of the 0.6-V micropower LNA is depicted in Fig. 17. The circuit design starts with the device size and bias point of the cascaded gain stages. For optimum circuit performance in terms of gain and linearity, the voltage V_P is designed at half of the supply voltage, specifying the aspect ratios of gain stages M_1 , M_2 , and M_3 as

$$\left(\frac{W}{L}\right)_1 : \left[\left(\frac{W}{L}\right)_2 + \left(\frac{W}{L}\right)_3\right] = \mu_p : \mu_n \quad (52)$$

where μ_n and μ_p are the mobility of the nMOS and PMOS, respectively. Once the device size and bias point of each stage are determined, the input matching network is accomplished by selecting the values of L_1 and L_2 for simultaneous gain and noise matching. On the other hand, the values of the LC networks including inductors $L_3 - L_7$ and capacitors $C_1 - C_3$ are designed for power matching in between the gain stages. For optimum circuit performance, iterations may be required in the design procedure. The final circuit parameters of the proposed LNA are tabulated in Table I.

Fig. 18 shows a microphotograph of the fabricated LNA with a chip area of $0.86 \times 1.1 \text{ mm}^2$ including the pads. In this design, 3-D spiral inductors utilizing multiple interconnection layers are employed for the source degeneration and the interstage matching to minimize the chip size. Meanwhile, the inductor L_1 at the LNA input is realized by a planar structure with a high quality factor for minimum noise figure. Operated at a supply voltage of 0.6 V, the LNA consumes a dc power of 900 μW .

Fig. 21. Design flow of the proposed complementary current-reused mixer.

The small-signal characteristics of the fabricated circuit are demonstrated in Fig. 19. Due to the use of the cascaded gain stages, the LNA exhibits a linear gain of 9.2 dB at the center frequency of 5 GHz with a 3-dB bandwidth of 1 GHz. The relatively flat gain response allows wideband applications for frequencies from 4.5 to 5.5 GHz. With the on-chip matching networks, the input and output ports are matched to 50 Ω in the vicinity of the center frequency. The measured $|S_{11}|$ and $|S_{22}|$ at the center frequency are -12 and -21 dB, respectively. The noise figure of the LNA was measured without external noise matching, exhibiting a minimum value of 4.5 dB at 5 GHz. To evaluate the large-signal behavior of the LNA, $P_{\text{in-1 dB}}$ and

TABLE III
CIRCUIT PARAMETERS OF THE MIXER

Devices	Design Values
M_1	92.5 μm / 0.18 μm
M_2	40 μm / 0.18 μm
M_3	40 μm / 0.18 μm
L_1	3.8 nH
L_2	0.3 nH
L_3	1.7 nH
C_1	1.0 pF
R_1	380 Ω
R_L	1 k Ω

Fig. 22. Microphotograph of the fabricated mixer.

IIP₃ were characterized by the two-tone harmonic measurement with 20-MHz input frequency spacing. Fig. 20 shows the measured results with $P_{\text{in-1 dB}}$ of -27 dBm and IIP₃ of -16 dBm at the 5-GHz frequency band.

The performance of the fabricated LNA is summarized in Table II along with previously published data [21]–[23] for comparison. It is noted that the proposed LNA exhibits the lowest power consumption and supply voltage while maintaining competitive performance in terms of gain and noise figure at 5 GHz. A widely used figure of merit, gain/power quotient, is also adopted for the performance evaluation. In this design, a gain/power quotient of 10.2 dB/mW is achieved. To the authors' best knowledge, this is the highest record that has ever been reported in standard CMOS technologies.

In this particular design, the LNA performance in terms of the linearity and noise figure are degraded to some extent compared with the conventional circuit implementations. However, for most of short-range communication systems, the physical (PHY) layer specifications are not as stringent [24]. Instead, the fabrication cost and power consumption are major concerns. Therefore, the proposed circuit techniques are well suited for such wireless applications at multigigahertz frequencies.

B. Down-Conversion Mixer

Fig. 21 shows the simplified design procedure of the ultra-low-voltage down-conversion mixer. The circuit design

Fig. 23. Measured (solid line) and simulated (dotted line) conversion gain of the mixer versus LO power level.

Fig. 24. Measured (solid line) and simulated (dotted line) input reflection coefficient of the mixer.

Fig. 25. Two-tone harmonic measurement of the 5-GHz mixer with an input frequency spacing of 20 MHz.

starts with the device size and bias point of the transistors M_1 in the transconductance stage. In order to maximize the IIP₃ of the mixer, it is desirable to design the sweet spot at a gate voltage of the supply voltage while maintaining the required input matching at the RF input. Note that the performance of the mixer is strongly influenced by the current-bleeding ratio. A tradeoff has to be made among the conversion gain, noise figure, and linearity for the mixer design. Once the values of

TABLE IV
PERFORMANCE COMPARISON OF LOW-VOLTAGE AND LOW-POWER MIXERS

	Unit	This Work	[25]	[26]	[27]	
Technology	—	0.18- μm CMOS	0.35- μm CMOS	0.18- μm CMOS	0.13- μm CMOS	
RF/LO/IF Frequency	GHz	5.2 / 5.1 / 0.1	0.9 / 0.8 / 0.1	2.401 / 2.4 / 0.001	2.51 / 2.5 / 0.01	
LO Power	dBm	-2	-12	—	-1	
Supply Voltage	V	0.6	0.9	1.0	0.8	0.6
DC Power	mW	0.8	4.7	3.2	2.4	1.6
Conversion Gain	dB	3.2	2.0	11.9*	5.7	5.4
Input Matching	dB	-12.0	—	—	—	
$P_{\text{in-1dB}}$	dBm	-15.0	-8.0	—	-6.5	-9.2
IIP_3	dBm	-8.0	3.5	-3	4.3	-2.8
Noise Figure	dB	14.0 (DSB)	13.5 (SSB)	13.9 (SSB)	15.9 (SSB)	14.8 (SSB)
Isolation (LO-RF/LO-IF)	dB	> 30	—	—	> 50	

* voltage gain

R_1 and R_L are determined, the aspect ratio of commutating stage $M_2 - M_3$ is chosen such that complete current switching is ensured for the specified LO power level. Similar to the LNA design, iterations may be required to achieve the desirable circuit performance, and the final design values for the 5-GHz down-conversion mixer are summarized in Table III.

Fig. 22 shows a microphotograph of the fabricated mixer with a chip area of $0.95 \times 0.7 \text{ mm}^2$. The RF port of the mixer is matched to 50Ω with the source degeneration, and the gate voltage of M_1 is provided externally via a bias tee. In order to drive the $50\text{-}\Omega$ load, the open-source buffer is also employed. To convert the differential signals into a single-ended one, an external power combiner was employed at the IF output. All losses from the adaptors, cables, and power combiners in the measurement setup were calibrated and deembedded in the experimental results. Biased at a reduced supply voltage of 0.6 V, the power consumption of the mixer core is $792 \mu\text{W}$.

With an RF input at 5.2 GHz and an LO frequency of 5.1 GHz, the measured down-conversion gain versus the LO power is illustrated in Fig. 23, indicating a maximum gain of 3.2 dB at an LO power of -2 dBm . The moderate conversion gain of the mixer is mainly due to the limitations on the supply voltage and power consumption. For a fixed IF of 100 MHz, measurement of the down-conversion gain versus the RF frequency was performed, and a 3-dB bandwidth of 1.6 GHz is demonstrated. Due to the use of source degeneration at the RF port, good input matching is achieved. As shown in Fig. 24, the RF return loss in the vicinity of 5 GHz is generally better than 10 dB. In addition, the port-to-port isolations were also characterized, and the obtained LO-to-RF and LO-to-IF isolations are higher than 30 dB. Another important specification in the mixer design is the noise figure. Based on the experimental results, a double-sideband noise figure of 14 dB is achieved at an RF frequency of 5.2 GHz. In order to evaluate the circuit linearity, a two-tone harmonic measurement with a frequency spacing of 20 MHz was carried out. Fig. 25 shows the measured intermodulation distortion versus the input power sweep, indicating a $P_{\text{in-1 dB}}$

of -15 dBm and an IIP_3 of -8 dBm at the 5-GHz frequency band.

Table IV summarizes of the performance of the proposed mixer along with the results from the previously published data [25]–[27] for comparison. As indicated in Table IV, the designed circuit reveals the lowest power consumption and supply voltage for active mixers while maintaining a reasonable conversion gain at 5-GHz frequency band.

VI. CONCLUSION

In this paper, complementary current-reused circuit techniques suitable for the design of RF frontends has been demonstrated. Theoretical analysis and design tradeoffs have been presented for the circuit implementations based on a semiempirical MOSFET model. Using a standard 0.18- μm CMOS process, an LNA and down-conversion mixer have been designed and fabricated at the 5-GHz frequency band. With the proposed circuit topologies, the RF frontend circuits can operate at a reduced supply voltage of 0.6 V with power consumption less than 1 mW, exhibiting a great potential for applications in ultra-low-power and ultra-low-voltage wireless systems.

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