A W-Band Medium Power Amplifier in 90 nm CMOS

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Abstract—A W-band CMOS medium power amplifier (PA) is presented in this letter. The circuit is implemented in 90 nm mixed signal/radio frequency CMOS process. By utilizing balanced architecture, the PA demonstrated a measured maximum small signal gain of 17 dB with 3 dB bandwidth from 91 to 108 GHz. The saturation output power (\(P_{\text{sat}}\)) is 12 dBm between 90 and 100 GHz for \(V_{\text{ds}}\) of each transistor at 1.5 V. To our knowledge, this is the highest frequency CMOS PA to date.

Index Terms—CMOS, microwave monolithic integrated circuit (MMIC), power amplifier (PA), W-band.

I. INTRODUCTION

The W-band (75–110 GHz) frequencies have been used for many military and civil applications. W-band power amplifiers (PAs) have been demonstrated using GaAs and InP-based HEMT monolithic microwave integrated circuit (MMIC) processes [1]–[3] with very good output power performances. On the other hand, Si-based MMICs (SiGe BiCMOS and CMOS) demonstrated the performances in millimeter-wave (MMW) regime recently [4]–[10], but output power is still a bottleneck in the transceiver components due to the limited breakdown voltage of CMOS transistors. The best CMOS PAs at W-band is operated at 77 GHz with 6.3 dBm output power [7].

This letter presents a medium power covering 90 to 108 GHz in 90 nm CMOS technology. This PA achieves a maximum linear gain of 15.1 dB at 100.5 GHz when each transistor \(V_{\text{ds}}\) is biased at 1.2 V, with a \(P_{\text{sat}}\) of 10 dBm and \(P_{1\text{dB}}\) of 6 dBm. A \(P_{\text{sat}}\) of 12 dBm is obtained if \(V_{\text{ds}}\) was increased to 1.5 V, and it demonstrates an \(P_{1\text{dB}}\) of 8 dBm and a maximum linear gain of 17 dB at 102.6 GHz.

II. CIRCUIT DESIGN

The W-band PA is fabricated in commercial standard bulk 90 nm 1P9M CMOS process, which provides one poly layer for the gates of CMOS transistors and nine metal layers with ultra-thick top metal (metal 9) of 3.3 \(\mu\)m. A RF NMOS of 2 \(\mu\)m 20 fingers transistor at 1.2 V bias has the maximum frequency of oscillation (\(f_{\text{osc}}\)) of 150 GHz. Passive elements including metal-insulator-metal (MIM) capacitors are available between metal 8 and metal 7 [11].

The PA is essentially a three-stage design with a first stage single-ended amplifier to drive a two-stage balanced amplifier, as the block diagram shown in Fig. 1. We utilized balanced structure to achieve twice of the output power. In addition, the balanced structure cancels reflected powers of the two amplifier branches and improves the overall amplifier return loss. The schematic of the complete PA is shown in Fig. 2. Cascode NMOS is used in each stage for higher gain. The device size of the RF NMOS transistor is selected to be 20 fingers with each finger length of 2 \(\mu\)m. Thin-film microstrip (TFMS) lines were used for the matching circuits and all of the interconnections to reduce the chip size, as many reported MMW CMOS circuits [11], [12]. The passive elements were simulated using the full-wave EM simulator Sonnet [14] and the complete circuit simulation was performed using Agilent ADS. Fig. 3 shows the chip photo of the PA. The chip size is 0.4 mm\(^2\), including all testing pads and dummy metal.

III. MEASURED RESULTS

The CMOS medium PA was measured through on-wafer probing. The small signal gain and input/output return losses of the PA with different drain biases are plotted in Figs. 4 and 5. When each transistor \(V_{\text{ds}}\) is biased at 1.2 V with \(V_{\text{gs}}\) set to 0.8 V, a measured maximum small signal gain of 15.1 dB is achieved at 100.5 GHz with 3 dB bandwidth of 18 GHz from 90 to 108 GHz. The input return loss is better than 7 dB through the entire W-band. Owing to the balanced design of the output stage, the PA achieves good output return loss of better than 15 dB. The PA demonstrates an output power of 10 dBm with about 7 dB saturated power gain, and the 1-dB compression point \((P_{1\text{dB}})\) occurs at 6 dBm from 90–100 GHz.

We also measured the PA with each transistor \(V_{\text{ds}}\) raised to 1.5 V. A peak linear gain of 17 dB at 102.6 GHz is achieved with the same 3-dB BW. The input and output return losses
are better than 6 and 14 dB through the W-band, respectively. It demonstrates an output power of 12 dBm with 9 dB power gain, and the 1-dB compression point ($OP_{1,\text{dB}}$) occurs at 8 dBm from 90–100 GHz. Fig. 6 plots $P_{\text{out}}$, gain, and PAE versus $P_{\text{in}}$ at 94 GHz for both 1.2 and 1.5 V $V_{\text{ds}}$ bias conditions.

The saturated output powers ($P_{\text{sat}}$) with respect to different frequencies and different drain biases are plotted in Fig. 7. This PA shows a wideband characteristic because of using balanced structure. To the author’s knowledge, this PA is the first CMOS PA demonstrated above 100 GHz frequencies.

**IV. CONCLUSION**

In this letter, we reported a W-band three-stage cascode medium PA using 90 nm CMOS process. A small signal gain of 17 dB from 90 to 108 GHz and a maximum output power of 12 dBm between 90 and 100 GHz have been achieved.
This work is the highest frequency CMOS PA demonstrated to date.

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REFERENCES


