A Low-Power 114-GHz Push–Push CMOS VCO Using LC Source Degeneration

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Abstract—An LC source-degeneration negative-resistance cell of an LC VCO is investigated, which is capable of operating at millimeter-wave (MMW) range with low dc power consumption. Several negative-resistance cells in LC oscillators are also compared. The LC source-degenerated topology is demonstrated through a 114-GHz push-push fully integrated LC VCO implemented in TSMC 0.13- μm CMOS process. With core power consumption of 8.4 mW, the tuning range at the fundamental port is 56.4–57.6 GHz and at the push-push port is 112.8–115.2 GHz. The measured phase noise at the fundamental port is -113.6 dBc/Hz at 10-MHz offset. This VCO is believed to have the best figure of merit among MMW VCOs using bulk CMOS processes.

Index Terms—CMOS, millimeter-wave (MMW), negative-resistance cell, voltage-controlled oscillators (VCOs).

I. INTRODUCTION

MILLIMETER-WAVE (MMW) voltage-controlled oscillators (VCOs) are key components in advanced communication and sensor systems. Potential applications which require oscillation frequencies in the MMW band include 60-GHz WLAN and automotive radar systems. In the past decades, MMW VCOs were realized in III-V compound devices or SiGe HBT [1]–[5]. Not until recently have MMW VCOs been realized in CMOS technology [6]–[18]. Due to the inherently lower unit current–gain frequency (f_T) and maximum oscillation frequency (f_{max}) of CMOS devices as compared to III-V compound devices or SiGe HBT, it is crucial to investigate the high-frequency behavior of a negative-resistance cell when designing MMW CMOS VCOs. Only recently has the issue about the frequency limitation of a cross-coupled negative-resistance cell been noticed [19]. Also, new circuit topologies have been proposed to overcome this problem [20]–[23].

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In [19], the maximum attainable oscillation frequency was proposed to show the limitation of a cross-coupled pair when oscillation frequencies approaches f_T . The analysis was further investigated and extended to different technologies [22]. Afterwards, several schemes were devised to extend the maximum attainable oscillation frequency beyond that of a cross-coupled pair; all were realized successfully with bipolars and are based on cascading an emitter follower with an active device to provide capacitive emitter degeneration [20]–[23]. However, because of the inherently lower g_m of CMOS devices, negative-resistance cells proposed in [20]–[23] require larger device sizes and hence higher power consumption when applied in CMOS technology.

In this paper, we show that an LC source-degeneration negative-resistance cell has a better frequency response to operate at MMW range under low power consumption. The push-push principle was also employed to obtain an output frequency beyond f_{max} [12]. A low-power 114-GHz push-push VCO [17] was designed, implemented, and measured, which shows the best figure of merit (FOM) among MMW VCOs using bulk CMOS process.

This paper is organized as follows. In Section II, several negative-resistance cells are compared; their limitations to operate at high frequency using CMOS technology are also discussed. Then, the analysis of the LC source-degenerated negative-resistance cell will be given. It will be shown that this topology can operate at high frequencies under low dc consumption. Design issues and circuit implementations are described in Section III. Section IV presents the measurement results of the 114-GHz push-push VCO for verification.

II. CIRCUIT CONCEPT

A. Technology Description

The VCO was designed and fabricated in TSMC 0.13- μm mixed-signal/RF CMOS technology featuring a metal stack with one poly layer and eight copper metal layers. The thickness of the top metal is 2 μm for the realization of inductive transmission lines. When biased at class-A operation, the six-finger device with V_{th} of 0.44 V and total gate width of 12 μm yields an f_T and an f_{max} of 85 and 90 GHz, respectively. In this paper, all of the analysis and comparisons are based on this MOS device. The simplified small-signal equivalent circuit of a typical n-channel field-effect transistor (FET) is shown in Fig. 1. The parasitic inductors are neglected here because of the small inductance.

Fig. 1. Simplified small-signal equivalent circuit of nMOS with total gate width of 12 μm at $V_{gs} = 0.75$ V, $V_{ds} = 1.2$ V, and $I_{ds} = 3.5$ mA.

Fig. 2. (a) Parallel *LC* oscillator model. (b) Cross-coupled negative-resistance cell.

B. Analysis of Circuit Topologies

Although oscillation is a large-signal behavior, small-signal analysis still provides insight for preliminary design. A simplified circuit model for a parallel *LC* oscillator is shown in Fig. 2(a), where R_p represents the tank loss plus the loss of output buffers, and R_x and C_x represent the effective negative resistance and capacitance generated by the active devices. To satisfy the small-signal oscillation condition, the magnitude of the effective negative resistance $|R_x|$ should be smaller than R_p . The most commonly used negative-resistance cell is a cross-coupled pair [Fig. 2(b)] for its simplicity and differential signaling. In [19], Veenstra proposed the maximum *attainable* oscillation frequency (f_{trans}), which is defined as the frequency where the resistance R_x turns from negative to positive. Then, in [22], Jung revisited the issue and compared the difference between bipolar and CMOS devices. The cross-coupled pair has the limitation of a fixed f_{trans} under a fixed device size and biasing condition. Also, as the oscillation frequency approaches f_{trans} , R_x drops rapidly, making the value of $|R_x|$ even larger than R_p such that stable oscillation cannot be satisfied.

Fig. 3. CMOS versions of the negative-resistance cells proposed in (a) [20] and (b) [22].

Veenstra and Jung proposed other implementations of negative-resistance cells to increase f_{trans} [20]–[23]. Their topologies were realized successfully with bipolars and are based on cascading an emitter follower with an active device to provide capacitive degeneration. We now investigate the two topologies in TSMC 0.13- μm CMOS technology, as shown in Fig. 3. Under the same device size (six-finger NMOS, with $W/L = 12 \mu\text{m}/0.13 \mu\text{m}$) and bias condition (3.5 mA per transistor) as those of the cross-coupled pair, the simulated R_x 's are given in Fig. 4. In BJT implementations, the two topologies can achieve higher f_{trans} 's than that of a cross-coupled pair; however, in CMOS, the cross-coupled pair outperforms the two topologies under the same device size and bias condition. The f_{trans} of a cross-coupled pair is higher in CMOS than those in BJT implementations because of the lower gate resistance of CMOS devices [22]. Moreover, combined with another factor—the inherently lower g_m of CMOS devices, the two topologies instead have larger $|R_x|$'s than a cross-coupled pair before the transition frequency. This can be inferred from the equations of R_x 's as functions of frequency and device parameters for a cross-coupled pair [19], the topology proposed by Veenstra [20], and the topology proposed by Jung [22]. Hence, the two topologies are more difficult to be implemented in CMOS since higher R_p (i.e., higher quality factor of the tank) is required to satisfy the oscillation condition. To improve the $|R_x|$'s, larger device size must be used for a larger g_m . However, higher power consumption is required; also, the f_{trans} will be degraded due to the larger parasitic capacitance. Therefore, we were motivated to develop a negative-resistance cell for high-frequency oscillation suitable in CMOS technology under low power consumption.

Negative-resistance cells based on capacitive degeneration have been widely used [24]–[30]. The Colpitts and Clapp (or Clapp–Gouriet) oscillators are of this kind [25]. It is pointed out that emitter (source) capacitive degeneration can avoid the tradeoff between oscillation frequency and power consumption

Fig. 4. Simulation results of R_x 's for different negative-resistance cells in 0.13- μm CMOS technology.

Fig. 5. (a) Colpitts and (b) Clapp (or Clapp-Gouriet) oscillators.

[30]. Also, it has a higher transition frequency of negative resistance and a smaller parasitic capacitance [20], [22]. However, the degenerating capacitors implemented with cascading stages [20]–[22] will require higher supply voltage and contribute more noise.

Fig. 5 presents Colpitts and Clapp oscillators. The tuning capacitor can be placed either at the gate (base) [26], [27] or at the source (emitter) [28], [29]. Both topologies can be analyzed by separating the negative-resistance cell at the gate (base). The *series* negative resistance looking into the gate (base) can be approximated as $-g_m/\omega^2 C_1 C_2$ [25], while the *parallel* negative resistance R_x was derived in [22]. However, the two equations do not take all the parasitic effects into account and hence do not predict the transition frequency. From simulations results, the f_{trans} 's of the R_x 's of Colpitts and Clapp oscillators can be designed to be higher than that of a cross-coupled pair with proper values of C_1 and C_2 . However, the R_x 's and f_{trans} 's are severely affected by the output load Z_L . Thus, the design of the output buffer stage is critical to the oscillator performance [28], [29].

Fig. 6. (a) Schematic of the LC source-degenerated negative-resistance cell. (b) The differential form of (a).

Fig. 6(a) shows the LC source-degenerated negative-resistance cell [26], [28], [29] based on the equivalent circuit of a YIG oscillator [31]. It consists of a source resonator (C_s and L_s) and a common-gate inductor L_g . The source capacitor C_2 in Colpitts and Clapp oscillators is replaced with an LC source resonator, allowing biasing current drift through L_s to ground and saving the supply voltage. In this topology, the tank is placed at the drain and the negative resistance is analyzed looking into the drain of the transistor. This configuration will be shown to have a better characteristic for a low-power MMW CMOS VCO design.

The differential form for implementing the push-push VCO is shown in Fig. 6(b). The odd-mode input resistance R_x is equal to that of its half circuit as in Fig. 6(a). Referring to the small-signal equivalent circuit in Fig. 1 where the body is connected to the source, and neglecting R_i (the relatively small resistance), R_d , and C_{pd} (they can be absorbed into R_p and C_p), and C_{pg} (it forms a parallel LC tank with L_g and the reason will be explained later), the negative resistance R_x looking into the drain of the transistor can be derived as

$$R_x = 1/\text{Re}[Y_{\text{in}}] \quad (1)$$

where

$$Y_{\text{in}} = \frac{1/Z_d + sC_{gd}(1+H)}{1 + (R_s + Z_s)(g_m + 1/Z_d - sC_{gs}H)} \quad (2)$$

$$H = \frac{(g_m - sC_{gd})(R_g + sL_g) + (g_m + 1/Z_d)(R_s + Z_s)}{s(C_{gs} + C_{gd})(R_g + sL_g) + 1 + sC_{gs}(R_s + sC_{gd})} \quad (3)$$

$$Z_s = \frac{1}{1/sL_s + sC_s} = \frac{sL_s}{1 - \omega^2 L_s C_s} \quad (4)$$

$$Z_d = \left(\frac{1}{R_{ds}} + sC_{ds} + \frac{1}{R_{bx} + 1/sC_{bx}} \right)^{-1} \quad (5)$$

As L_g must be chosen to be sufficiently large to avoid four zeros of the denominator of $\text{Re}[Y_{in}]$, which will cause $|R_x|$ to be too large to be impractical, $\text{Re}[Y_{in}]$ has two roots at

$$\omega_1 \approx \frac{1}{\sqrt{L_s C_s}} \quad (6)$$

$$\omega_2 \approx \sqrt{\frac{A + B + C + \sqrt{(A + B + C)^2 - 4AB}}{2AB}} \quad (7)$$

where

$$A = (C_{gs} + C_{gd})L_g, \quad (8)$$

$$B = C_s L_s \quad (9)$$

$$C = C_{gs} L_s. \quad (10)$$

R_x has two transition frequencies at ω_1 and ω_2 . Note that the C_{gs} and C_{gd} are usually smaller than C_s by a factor of 10. We have to design $\omega_1 < \omega_2$ for practical values of L_g , L_s , and C_s . With the device parameters in Fig. 1 and $C_s = 0.1$ pF, we can plot the analytical results of R_x for different values of L_s and L_g , as shown in Fig. 7(a). The circuit simulation results of R_x are given in Fig. 7(b). From Fig. 7, (6), and (7), we have two observations.

- 1) The R_x of the negative-resistance cell is negative between the two transition frequencies ω_1 and ω_2 . This is because, when the frequency is higher than the resonance frequency of the source resonator ω_1 , the source resonator exhibits a capacitance for positive feedback. However, when the frequency is higher than ω_2 (approximately the resonance frequency of the parallel *LC* tank at the gate of the transistor formed by L_g and the input parasitic capacitance at the gate to ground), there is no longer inductance at the gate for destabilization. Hence, the R_x turns from negative to positive again. Since we neglected C_{pg} in our analysis, the ω_2 in the analytic result is higher than the ω_2 in the simulation result.
- 2) The two transition frequencies ω_1 and ω_2 can be chosen to be the desired frequencies by properly selecting the values of L_g , L_s , and C_s without changing the biasing condition.

These two properties make the negative-resistance cell advantageous in a low-power MMW CMOS VCO design since, under a given power budget, the oscillation frequency of the VCO is not limited to a fixed transition frequency and can be designed to be higher than conventional negative-resistance cells.

Fig. 8 is the comparison of the R_x 's of a cross-coupled, Colpitts, and the *LC* source-degenerated negative-resistance cells using the same device size and under the same bias condition. Choosing C_1 and C_2 in the Colpitts negative-resistance cell to be 0.1 pF and $Z_L = 0$, the f_{trans} of the Colpitts cell can be higher than that of the cross-coupled pair. However, the f_{trans} of the Colpitts cell will degrade as Z_L changes to other impedances. For example, as the Z_L is 50 Ω , the f_{trans} degrades to 73 GHz. On the other hand, the *LC* source-degenerated negative-resistance cell has a smaller $|R_x|$ than those of the other two in the frequency range of interest.

Fig. 7. Plots of negative resistance R_x for different L_s . (a) Analytical results. (b) Simulation results.

III. CIRCUIT IMPLEMENTATION

A 114-GHz push-push VCO is implemented based on (6) and (7) using 0.13- μm CMOS process. First, the first transition frequency ω_1 was calculated. For an oscillation frequency centered at 57 GHz, according to (6) and Fig. 7, ω_1 has to be set around 50 GHz, i.e., the resonance frequency of L_s and C_s is around 50 GHz. However, from (8), the value of L_s affects ω_2 as well. Fig. 9 shows the circuit simulation results of R_x under a fixed value of L_g (0.4 nH) and a fixed resonance frequency of the *LC* source resonator (50 GHz) using ideal capacitor and inductors. We can see that a higher value of L_s results in higher ω_2 . To guarantee the safe range of the negative resistance around 57 GHz, we chose $C_s = 0.1$ pF and $L_s = 0.1$ nH, giving $\omega_2 = 68$ GHz. All of the inductors in this VCO are implemented with thin-film microstrip lines, as shown in the cross section of Fig. 10(a). The distance from the signal (Metal 8) to ground (Metal 1) is the height of the oxide (5 μm), so the lines can be laid out as compact meanders to minimize the chip size. On the other hand, using coplanar waveguides (CPWs) to implement inductors would occupy a larger area, though CPWs can provide higher quality factor and larger metal width in this

Fig. 8. Comparison of R_x 's between the cross-coupled pair, Colpitts, and the LC source-degenerated negative-resistance cells.

Fig. 9. Circuit simulation results of the R_x 's for different values of L_s with fixed value of L_g (0.4 nH) and ω_1 (50 GHz).

process. The characteristic impedances and the required length of the microstrip lines were roughly calculated using conventional transmission-line equations and were then verified by the electromagnetic field simulator Sonnet [32]. The minimum line width, given by the maximum tolerable current density, has been chosen for the upper metallization layer in order to minimize the line length. In this process, the thin-film microstrip line of 50- Ω characteristic impedance is about 10 μm . The L_s and L_g are optimized as 2.5 μm wide ($Z_0 = 92 \Omega$) for physical length and quality factor [17.9 at 57 GHz, as given in Fig. 10(b)].

Next was the selection of L_g . Fig. 11 presents the simulation results of R_x and C_x for different values of L_g . As revealed from (7), for fixed values of L_s and C_s , decreasing the value of L_g leads to higher ω_2 . However, $|R_x|$ degrades as well. Hence, a higher value of L_g is preferable for R_x , as long as ω_2 guarantees the safe range of the negative resistance around 57 GHz. As for C_x , interestingly, the LC source-degenerated negative-resistance cell shows inductive impedance around 58 GHz when

Fig. 10. (a) Cross-sectional view of the thin-film microstrip line. (b) Quality factor of the thin-film microstrip line with line width of 2.5 μm and length of 550 μm .

$L_g = 0.6$ nH. This means that it is possible to design a parasitic-free [22] negative-resistance cell in the desired band, i.e., it is possible to achieve a very wide tuning range. However, since the self-resonance frequency of a 0.6-nH transmission line is below 57 GHz, we chose the value of L_g to be 0.4 nH, whose length is 550 μm . Now the selection of L_s , C_s , and L_g is completed, and the resulting R_x and C_x at 57 GHz are -342Ω and 14.2 fF, respectively.

Finally, we designed the tank and the push-push VCO. Fig. 12 is the schematic of the VCO. The lower part is the LC source-degenerated negative-resistance cell in differential form and the upper part is the LC tank. The gates of the transistors (M_1, M_2) are biased with a resistor R_g , and the supply voltage is fed through a 114-GHz quarter-wavelength short stub and the bias current drifts through L_s to ground. The tuning capacitors ($C_{\text{var}1}, C_{\text{var}2}$) were implemented with six-finger nMOS varactors, which were laid out as multifingers to reduce the gate resistance. The values of L_{d1} and L_{d2} were selected to make the overall imaginary part zero at 57 GHz. Combining $C_{\text{var}1}, C_{\text{var}2}, L_{d1}, L_{d2}$ (with the same quality factor of L_s and L_g) and the two common source output buffers, the resulting R_p at 57 GHz is 709 Ω , which is two times to $|R_x|$,

Fig. 11. Simulation results of (a) R_x and (b) C_x for different values of L_g with fixed values of L_s and C_s .

guaranteeing a safe oscillation condition. Fig. 13(a) shows the simulated odd-mode analysis after considering nonideal effects of MIM capacitors and thin-film microstrip lines by EM simulators. Since our analysis is based on the parallel *RLC* model and *Y*-parameters, here we observe the total conductance and susceptance of the oscillator. This is different from our approach in [17], which is based on *Z*-parameters. At 57 GHz, the total conductance of the overall circuit is negative, and the total susceptance is zero, guaranteeing the differential operation at fundamental oscillation frequency. On the other hand, to suppress the even-mode oscillation, the even-mode total conductance must be positive across the frequency range, i.e., the even-mode R_x should be designed to be positive. The even-mode R_x is related to R_g , which is only visible in even-mode operation, as shown in the schematic diagram at right-upper corner in Fig. 13(b). Thus, to suppress the even-mode oscillation of the push-push VCO, the value of R_g was designed at 1 $k\Omega$ such that even-mode R_x is positive across the frequency range. The chip photograph is illustrated in Fig. 14, with a chip size of 0.42 mm $\times$ 0.48 mm, including RF testing pads.

Fig. 12. Circuit schematic of the push-push CMOS VCO.

Fig. 13. Simulated (a) odd-mode and (b) even-mode VCO analysis.

Regarding the tuning range, the total capacitance seen by the varactors should be as small as possible to merit the tuning range of the varactors. In this design, the tuning range of this VCO was severely degraded due to the parasitic capacitance of the output buffers—which has to be added here to verify the fundamental oscillation. If a large tuning range is required in this case,

Fig. 14. Chip photograph (0.42 mm × 0.48 mm).

Fig. 15. Simulated (a) R_x and (b) C_x after C_s 's were replaced with varactors.

the C_s 's can be replaced with another varactor [28], [29] (and with control voltage V_{ctrl2}). For example, with C_s 's replaced with 48-finger nMOS varactors (gate width 96 μm and C_j from 75 to 165 fF) and other parameters unchanged, the simulated R_x and C_x are shown in Fig. 15(a) and (b). The originally designed C_x (14.2 fF) occurred at 57 GHz. After C_s 's are replaced

Fig. 16. Fundamental output frequency and power versus the control voltage from 0 to 1.2 V.

Fig. 17. Measured output spectrum at the push-push port before calibrating waveguide and probe losses.

with varactors, from Fig. 15(b), the desired C_x occurs from 52 to 61 GHz under different V_{ctrl2} 's. In this way, V_{ctrl2} acts as a coarse-tuning voltage while V_{ctrl1} acts as a fine-tuning one. Hence, a larger tuning range can be obtained. However, since we have focused the VCO design on its high-frequency performance, we did not replace the C_s 's with varactors here.

IV. MEASUREMENT RESULTS

This CMOS VCO is measured via on-wafer probing. The VCO starts to oscillate at a bias current of 2 mA at 0.7 V. Fig. 16 shows the measured output frequency and power versus the control voltage at the fundamental port. With V_G and V_{ctrl1} , the frequency tuning range at the fundamental port is 56.4–57.6 GHz and at the push-push port is 112.8–115.2 GHz. The limited tuning range is due to the parasitic capacitance contributed by the output buffers. Regarding the RF output power measurements, the VCO was measured via V-band/W-band spectrum analyzers and the results were verified by V-band/W-band power meters. The measured output spectrum of the push-push port before calibrating the waveguide and probe losses is shown in Fig. 17. After calibrating the waveguide and probes loss,

TABLE I
PREVIOUSLY REPORTED MMW CMOS VCOs

Ref.	Process	Center Frequency (GHz)	f_T (GHz)	f_{max} (GHz)	Topology	Output Power (dBm)	Phase Noise (dBc/Hz)	Phase Noise offset (MHz)	Core Power Consumption (mW)	F.O.M.
[7]	0.12- μ m CMOS SOI	31	150	230	Ring	-16	-75	1	4.5	-158.30
[8]	0.25- μ m CMOS	40	30	45	Cross-coupled and push-push	-15	-83	1	224	-151.54
[9]	0.13- μ m CMOS SOI	40	148	168	Complementary cross-coupled	-8	-97	1	11.3	-178.51
[10]	0.13- μ m CMOS	43	N/A	N/A	Cross-coupled	-24	-90	1	14	-171.21
[11]	Modified 0.25- μ m CMOS	50	25-30	N/A	Cross-coupled	-12.5	-100	1	13	-182.84
[12]	0.12- μ m CMOS	51	100	N/A	Cross-coupled	-30	-85	1	1	-179.15
[13]	0.18 μ m CMOS	52.5	N/A	N/A	LC type	-8	-86	1	41	-164.28
[14]	0.09- μ m CMOS SOI	60	150	160	Cross-coupled	-6.8	-89	1	21	-171.34
[15]	0.25- μ m CMOS	63	30	45	Cross-coupled and push-push	-4	-85.3	1	118.1	-160.56
[16]	0.09- μ m CMOS	100	N/A	110	Optimum pumping	-65	-85	10	30	-150.23
[18]	0.09- μ m CMOS	131	120	142	Cross-coupled and push-push	> -28.6	-108.4	10	21	-177.52
This Work	0.13- μ m CMOS	114	85	90	LC source degeneration and push-push	>-22.5	-107.6	10	8.4	-179.50

Fig. 18. Measured phase noise of the fundamental port at 56.7 GHz. The resolution bandwidth is 910 kHz and the video bandwidth is 10 kHz.

Fig. 19. Measured phase noise at the fundamental port versus the control voltage.

the measured output power is -5 dBm at fundamental port of 57 GHz and -22.5 dBm at push-push port of 114 GHz. Since the output frequency at the push-push port is higher than W-band test set, the real output power at the push-push port should be better than -22.5 dBm. The fundamental rejection at the push-push port is better than 15 dB. The core power consumption is 8.4 mW with 7 mA from a 1.2-V supply, and the output buffers consume 4.8 mW. Fig. 18 shows that the measured phase noise at 56.7 GHz is -113.6 dBc/Hz at 10-MHz offset, and the phase noise at the push-push port is expected to be 6 dB higher. The measured phase noise versus control voltage is shown in Fig. 19. The phase noise is almost the same within the control voltage. However, the phase noise degrades as V_G is tuned from 1 to 0.7 V. This is because, under

the same supply voltage, the phase noise is traded off with the bias current [33]. A summary of measured performance and comparison with recently reported Si-based MMW VCOs is shown in Table I. This VCO demonstrates the best output power at frequencies higher than 100 GHz [16]–[18] and the best FOM among MMW VCOs using bulk CMOS processes [8], [10], [12], [13], [15]–[18].

V. CONCLUSION

We have presented a negative-resistance cell using source degeneration that is advantageous for low-power MMW CMOS VCO design. Under a given power budget, the oscillation frequency can be designed to be higher than conventional negative-resistance cells by properly selecting the values of inductors

and capacitors according to the equations for the first and second transition frequencies. This topology is demonstrated through a 114-GHz push-push VCO in a TSMC 0.13- μm CMOS process. The VCO is the first CMOS frequency source beyond 100 GHz and has the best FOM among MMW VCOs using bulk CMOS processes.

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