A 50 to 94-GHz CMOS SPDT Switch Using Traveling-Wave Concept

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Abstract—A fully integrated single-pole-double-throw transmit/receive switch has been designed and fabricated in standard bulk 90-nm complementary metal-oxide semiconductor (CMOS) technology. Traveling wave concept was used to minimize the insertion loss at higher frequency and widen the operating bandwidth. The switch exhibits a measured insertion loss of 2.7 dB, an input 1-dB compression point (input $P_{1\text{ dB}}$) of 15 dBm, and a 29-dB isolation at the center frequency of 77 GHz. The total chip size is only $0.57 \times 0.42 \text{ mm}^2$ including all testing pads. To our knowledge, this is the first CMOS switch demonstrated beyond 50 GHz, and the performances rival those monolithic microwave integrated circuit switches using standard GaAs PHEMTs.

Index Terms—Complementary metal-oxide semiconductor (CMOS) integrated circuits, millimeter-wave switches, metal-oxide-semiconductor field-effect transistor (MOSFET) switches.

I. INTRODUCTION

A HIGH-QUALITY microwave switch is a key building block of a radio frequency (RF) front end for time-division duplexing (TDD) communication systems. A switch with low insertion loss, high isolation, and required power handling capacity is demanded. For a high level of integration, the switch has to be integrated with the transceiver. The advantages of complementary metal-oxide semiconductor (CMOS) technology for RF and microwave control functions over GaAs are its low-cost structure and its integration potential of RF, intermediate frequency (IF), and baseband blocks on the same die. Owing to the continuous scaling down of the CMOS technology, RF/microwave building blocks have moved from low gigahertz to higher frequency applications [1], [2].

Recently, several CMOS T/R switches using series-shunt topology were published with good performances [3], [4]. However, due to the limitation of the CMOS process and circuit topology, their operating bandwidth are limited to low-gigahertz application. In [5], a 0.13- μm CMOS switch using an on-chip impedance transformation network has pushed the operating frequency up to 15 GHz and also improved the power handling capacity. A simple method using body-floating technique to increase the power handling capacity of a CMOS switch without increasing additional area is proposed in [6]. For high frequency applications, traveling wave concept is

used in 0.18- μm and 0.13- μm CMOS switches to extend the operating frequency to about 50 GHz [7], [8]. Nevertheless, for operating frequencies above 50 GHz, switches are mostly dominated by GaAs switches due to their high performances [9]–[12]. However, GaAs switches based on HEMT devices need negative control voltages which are not compatible with most portable systems. Moreover, GaAs switches are difficult to meet the requirements for low cost and high level integration system applications.

In this letter, a single-pole-double-throw (SPDT) switch implemented in bulk CMOS 90-nm technology is demonstrated. With the traveling wave concept, the operating frequency can be extended to 94 GHz. The switch also demonstrates competitive performances as compared to those of GaAs switches. This SPDT switch presents a measured insertion loss of less than 3.3 dB from 50 to 94 GHz with isolation higher than 27 dB. The measured input $P_{1\text{ dB}}$ is 15 dBm at the center frequency of 77 GHz.

II. CIRCUIT DESIGN AND ANALYSIS

Fig. 1 shows the circuit schematic of the SPDT traveling-wave switch. The SPDT switch is formed by connecting two distributed single-pole-single-throw (SPST) switches to a matching T-junction. The shunt transistors periodically load the inductive transmission line (line width = 3 μm) at an optimal length ($L_d = 90 \mu\text{m}$) to form a distributed switch. In the on-state, the inductive transmission lines with the loaded off-state capacitances form an artificial line to pass the RF signals. In the off-state, the shunt on-state resistance shorts the RF signal to ground. The matching T-junction is formed by 50- Ω transmission lines (line width = 12 μm), and which is used to transform the isolated terminal into high impedance while the RF signals pass to the other terminal. Moreover, in order to compromise between the insertion loss and isolation, four stages are adopted in this distributed switch design. In the conventional GaAs-based HEMT switch designs using traveling-wave concept, large chip areas for ground-via holes are needed, which will cause the parasitic inductances and degrade the RF performances in the high frequencies [9], [10]. In the CMOS process, the large ground via-hole can be omitted and the device layout is more compact [7], [8]. Therefore, the CMOS traveling-wave switches are more attractive.

The total gate width of the metal-oxide-semiconductor field-effect transistors (MOSFETs) used in this design is 16 μm . The on-state resistance ($V_g = 1 \text{ V}$) and off-state ($V_g = 0 \text{ V}$) capacitance of a FET are 22 Ω and 12 fF, respectively. The gate bias is applied through a large resistor (2 k Ω) to prevent RF signal leakage. It is also noted that in order to increase the power handling capacity, the floating-body technique is utilized in this design, similar to that in [6].

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Fig. 1. Circuit schematic of the 77-GHz SPDT switch.

Fig. 2. Cross section of the thin-film microstrip line in 90-nm CMOS technology.

Fig. 3. Simulated insertion loss of the thin-film microstrip line with line of 300 μm and width of 12 μm ($Z_0 = 50 \Omega$).

In this design, for the consideration of the system integration, the transmission line is implemented by thin-film microstrip line [13], [14]. Fig. 2 shows the cross section of the thin-film microstrip line used in 90-nm CMOS technology. The signal line and ground plane is realized by the top metal 9 and bottom metal 1, respectively. The top metal 9 was formed using ultra-thick metal with thickness of 3.4 μm to minimize the RF signal loss. Fig. 3 shows the simulated insertion loss of the thin-film microstrip line with a line length of 300 μm and a width of 12 μm ($Z_0 = 50 \Omega$), and the simulated insertion loss is 0.15–0.2 dB from 50 to 110 GHz.

III. MEASUREMENT

The SPDT switch was designed and fabricated in standard MS/RF 90-nm CMOS technology. The chip photo of this SPDT switch is shown in Fig. 4, and the overall chip size (including the testing pads) is only 0.57 mm $\times$ 0.42 mm. Without the large ground via-hole of a HEMT device, the CMOS switch could have a much more compact chip size than a GaAs PHEMT switch.

Fig. 4. Chip photo of the SPDT switch, and the total chip size is 0.57 $\times$ 0.42 mm².

(a)

(b)

Fig. 5. Simulation and measured S parameters of the SPDT switch. (a) Insertion loss (S_{21}) and input return loss (S_{11}). (b) Isolation (S_{31}).

RF performances of this SPDT switch were tested via on-wafer probing using 8510C network analyzer with millimeter-wave test set. Two-port S -parameters were calibrated to the probe tips using an SOLT calibration kit. Simulated and measured results are shown in Fig. 5. In Fig. 5(a), the measured insertion loss is 2.7 dB at center frequency of 77 GHz with input return loss better than -20 dB. The measured insertion loss also show a wideband performance of less than 3.3 dB from 50 to 94 GHz. The measured isolation is about 29 dB at 77 GHz, and is better than 27 dB from 50 to 110 GHz. The measured phase response and group delay of S_{21} are shown in

Fig. 6. Measured phase response and group delay at the thru-port.

Fig. 7. Measured output power versus input power at the thru-port of the SPDT at 77 GHz.

TABLE I
PERFORMANCES SUMMARY OF THE CMOS SPDT SWITCH
AND RECENTLY PUBLISHED GaAs HEMT SWITCHES

Ref.	Technology	Frequency (GHz)	Insertion loss (dB)	Isolation (dB)	Chip size (mm ²)
[9]	0.15- μ m GaAs HEMT	50-70	< 1.8	> 32	3.5
[10]	0.1- μ m GaAs HEMT	15-80	< 3.6	> 25	2.25
[11]	0.15- μ m GaAs HEMT	40-85	< 2	> 30	1.45
[12]	0.15- μ m GaAs HEMT	20-110	< 5	> 23	0.68
This work	90-nm CMOS	50-94	< 3.3	> 27	0.24

Fig. 6. It is observed that the switch has a linear phase variation and a flat group delay. The power performance is measured via a millimeter-wave signal generator with a PA module. Fig. 7 shows the measured output power versus input power from port 1 to port 2 in the on-state at 77 GHz, and the measured input $P_{1\text{ dB}}$ is about 15 dBm.

Table I shows the comparisons of this work and recently published monolithic microwave integrated circuit (MMIC) switches over the same frequency range. This CMOS SPDT switch shows competitive insertion loss and isolation perfor-

mances compared with those of GaAs HEMT switches while with a smallest chip size of 0.24 mm².

IV. CONCLUSION

A high performance SPDT switch using CMOS 90-nm technology has been designed, fabricated, and tested. With the traveling-wave concept, the operating frequency is extended to the W-band. The switch shows a wideband performance of insertion loss less than 3.3 dB from 50 to 94 GHz and isolation higher than 27 dB from 50 to 110 GHz. The measured input $P_{1\text{ dB}}$ is 15 dBm at the center frequency of 77 GHz. The total chip size is only 0.24 mm². To the best of our knowledge, this is the first CMOS switch demonstrated beyond 50 GHz, which rivals the MMIC switches in GaAs PHEMT technologies.

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