A 4-GHz Phase Shifter MMIC in 0.18-μm CMOS

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Abstract—This letter presents a tunable phase shifter implemented in a 0.18-μm CMOS process for monolithic microwave integrated circuit (MMIC) applications. By employing active inductors in the synthetic transmission line architecture, the phase shifter exhibits a wide phase control range, low insertion loss, and miniaturized chip area. Characterized by the S-parameter measurement, the fabricated circuit demonstrates an insertion loss less than 1.1 dB within the 360° phase shift while maintaining a return loss better than 10 dB from 3.5 to 4.5 GHz. Due to the absence of distributed elements and spiral inductors, the area of the phase shifter core is 400 × 200 μm². To the authors’ best knowledge, this is the smallest chip size ever reported for an analog phase shifter at this frequency band.

Index Terms—Active inductors, low insertion loss, regulated cascode, synthetic transmission lines, tunable phase shifters, wide tuning range.

I. INTRODUCTION

PHASE shifters are widely used to control the phase of the transmitted or received microwave signals for radar systems, smart antennas, and measurement instruments. Due to the stringent performance requirements on both active and passive components, most of the microwave phase shifters were implemented in III–V compound semiconductors. With recent advances in the fabrication technology, more and more monolithic microwave integrated circuits (MMICs) have been demonstrated in CMOS technologies [1], [2]. However, the substrate losses and the inferior Q-factors of the passive components still impede the realization of CMOS phase shifters at microwave frequencies. In consideration of the hardware cost and system integration, it is desirable to implement high-performance microwave phase shifters using a standard CMOS process.

A variety of circuit topologies have been proposed for the implementation of phase shifters [3]–[5]. The distributed phase shifter [6] with diode-loaded transmission lines is widely used due to its low power consumption and low insertion loss. The major drawback of the distributed approach is the considerably large chip area, especially for applications below 10 GHz. In order to reduce the circuit size, an ultra-compact phase shifter was reported by using spiral inductors to replace the required transmission line sections [7]. Though a smaller circuit size can be achieved, it suffers from higher insertion loss and limited phase shift. In this letter, a novel circuit topology is presented to alleviate the design restrictions by employing active inductors for the synthetic lines. The proposed phase shifter exhibits wide phase control range and low insertion loss while maintaining a miniaturized circuit size and low power consumption.

II. CIRCUIT DESIGN

The concept of a distributed phase shifter is to use a tunable synthetic transmission line to control the phase of the incident signal. For frequencies well below the Bragg frequency [8], the periodically loaded line, as shown in Fig. 1(a), can be treated as a synthetic transmission line. Note that the series inductance $L_s$ can be realized by either a high impedance line or a spiral inductor for circuit implementations. As the capacitance of the varactor varies, the equivalent electrical length of the synthetic line changes, resulting in a differential phase shift between the input and the output. Considering a single section in the periodic structure, the maximum possible differential phase shift is given by [9]

$$
\Delta \phi_I = 2\pi f_0 \left( \sqrt{L_s C_{p_{\text{MAX}}}^2} - \sqrt{L_s C_{p_{\text{MIN}}}^2} \right)
$$

where $C_{p_{\text{MAX}}}$ and $C_{p_{\text{MIN}}}$ are the maximum and minimum capacitance of the varactor, respectively, and $f_0$ represents the center frequency. With a typical value of $C_{p_{\text{MAX}}}/C_{p_{\text{MIN}}}$ for the varactor, the maximum phase shift provided by a single section is approximately 30°.

To achieve a more efficient phase tuning mechanism, an alternative synthetic line is proposed as shown in Fig. 1(b), where each section behaves as a transmission line with an electrical length of 270°. Assuming the inductance $L_p$ in this topology has a tuning range from $L_{p_{\text{MIN}}}$ to $L_{p_{\text{MAX}}}$, the synthetic line can be used as an analog phase shifter with a maximum possible differential phase shift of

$$
\Delta \phi_{II} = 2\pi f_0 \left( \sqrt{C_s L_{p_{\text{MAX}}}^2} - \sqrt{C_s L_{p_{\text{MIN}}}^2} \right)
$$

from a single section. For circuit implementations, the inductance $L_p$ is realized by active inductors with a regulated cascode.
topology [10] as shown in Fig. 2. Since the input impedance of an active inductor strongly depends on the bias current of $M_1$ and $M_2$, the equivalent inductance $L_p$ can be tuned over a wide range by controlling $I_1$ and $I_2$. Using a 0.18-$\mu$m CMOS process, the simulation results indicate that a large inductance ratio $L_{p,\text{max}}/L_{p,\text{min}}$ can be achieved without significant degradation in the $Q$-factors, providing a maximum phase shift of 60° from a single section.

Based on the proposed synthetic line architecture with active inductors, a phase shifter is designed for continuous phase tuning. To ensure the required 360° phase shift over a wide frequency range, a synthetic line consisting of eight sections is employed. Due to the compact circuit size and high-$Q$ factor of the active inductor, the proposed topology allows a high section number without causing significant increase in the insertion loss. Therefore, it is suitable for CMOS implementations where a lossy substrate is mandatory.

III. EXPERIMENTAL RESULTS

The phase shifter MMIC has been designed and implemented in a standard 0.18-$\mu$m CMOS process. In order to achieve a 360° phase shift over a wide frequency range, the active inductors are designed to provide sufficient inductance ratio $L_{p,\text{max}}/L_{p,\text{min}}$ in this particular design. Based on the simulation results, the $L_{p,\text{max}}$ and $L_{p,\text{min}}$ of the active inductors are 4.8 and 1.3 nH, respectively. Fig. 3 shows the simulated $Q$-factors of the active inductors and MIM capacitors. With the enhanced $Q$-factors of the active inductors, the insertion loss of the phase shifter is dominated by the on-chip capacitors. Fig. 4 shows the micrograph of the fabricated circuit. Due to the absence of distributed elements and spiral inductors, the area of the phase shifter core is $400 \times 200 \mu$m$^2$. On-wafer probing was performed to characterize the performance of the phase shifter.

When operating at the 4-GHz band with a differential phase shift of 160°, the phase shifter draws a dc current of 10.72 mA from a 1.8-V supply voltage. The measured insertion loss and return loss are illustrated in Fig. 5(a) while the differential phase shift is shown in Fig. 5(b). As indicated in Fig. 5(a) and (b), the

![Fig. 2. Schematic and the small-signal equivalent circuit of the regulated cascode active inductor.](image)

![Fig. 3. Simulated $Q$-factors of the active inductors and MIM capacitors.](image)

![Fig. 4. Die photograph of the fabricated phase shifter.](image)

![Fig. 5. Measured (a) $S_{21}$, $S_{11}$ and (b) differential phase shift of the phase shifter.](image)
phase shifter exhibits an insertion loss less than 1.1 dB and a return loss better than 10 dB from 3.5 to 4.5 GHz. The phase tuning is achieved by controlling the transistor bias currents, where $I_1$ acts as the coarse tuning and $I_2$ is used for fine tuning. At 4 GHz, the insertion loss and return loss over the 360° phase shift range is shown in Fig. 6. The average insertion loss of the phase shifter is 0.3 dB with a variation of ±0.8 dB, while the return loss better than 10 dB is observed within the entire range. The performance of the phase shifter is summarized in Table I.

![Graph showing measured $S_{21}$ and $S_{11}$ of the phase shifter with 360° differential phase shift at 4 GHz.]

**Table I**

Performance Summary of the Phase Shifter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18-μm CMOS</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>3.5 – 4.5 GHz</td>
</tr>
<tr>
<td>Phase range</td>
<td>&gt;360°</td>
</tr>
<tr>
<td>Insertion loss</td>
<td>0.3 dB ± 0.8 dB</td>
</tr>
<tr>
<td>Return loss</td>
<td>&gt;10 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>16 – 25 mW</td>
</tr>
<tr>
<td>Chip size (including pads)</td>
<td>600x400 μm²</td>
</tr>
</tbody>
</table>

IV. Conclusion

A synthetic line architecture with active inductors has been proposed for the implementation of microwave phase shifters. Using a 0.18-μm CMOS process, the eight-section phase shifter is designed and implemented. The fabricated circuit exhibits an insertion loss less than 1.1 dB and a return loss better than 10 dB within 360° phase shift from 3.5 to 4.5 GHz. It provides a promising solution to the implementation of low-cost and high-performance phase shifter MMIC in standard CMOS technology.

**References**


