Timing and data recovery circuit for high-speed optical storage drives

Y.-B. Luo and T.-D. Chiueh

Abstract: A new timing recovery circuit for high-speed optical storage drives is presented. The core of the timing recovery circuit is a mixed-signal-controlled oscillator (MSCO) which is controlled simultaneously by a digital signal and an analogue signal. With digital control, the MSCO can operate in a broad frequency range, with very high switching speed and flexibility. Within a small frequency step defined by a particular digital control word, an analogue control signal can then fine-tune the MSCO through a feedback loop. In addition, to accommodate the data-transition characteristics in the CD-ROM or DVD-ROM data, a new phase detector is proposed. The proposed IC also includes a frame synchronisation block and an eight-to-fourteen demodulation circuit for CD-ROM data recovery. The chip was fabricated in a 0.6- μm n-well SPTM CMOS process. The timing recovery circuit achieves an operating frequency range of 70–180 MHz and its acquisition time is much less than 1 μs while consuming only 85 mW from a 5 V power supply.

1 Introduction

Recently, optical storage drives have become standard devices in personal computers and other consumer products, e.g. CD-ROM drives, DVD-ROM drives, MP3 players and game machines. In order to provide quality and performance, high throughput rate and short seek time in an optical storage drive are essential. To increase the data rate, the rotational speed of the spindle motor in optical storage drives has gradually increased. The constant linear velocity (CLV) control scheme is no longer applicable because the rotational speed of the spindle motor changes abruptly when seeking data. In this case, the temperature of the motor can rise to an unbearably high level [1]. Consequently, in modern high-speed optical storage drives, the constant angular velocity (CAV) control technique with fixed rotational spindle-motor speed is necessary. When we use the CAV technique to control the spindle motor, the data rate varies depending on which portion of a disc is being read. For example, in 40X CD-ROM drives, the range of the data rate is 77.8–172.9 Mbit/s (18X to 40X). Thus, the timing recovery circuit in CAV-controlled optical storage drives must operate in a very wide frequency range. In addition to high data rate, short seek time in optical storage drives is also important. Accordingly, a fast-acquisition and wide-frequency-range timing recovery circuit is imperative for CAV-controlled high-speed optical storage drives.

In summary, the timing recovery circuit in high-speed optical storage drives should have the following characteristics:

- possess a fast-acquisition ability to decrease the seek time;
- operate in a wide frequency range according to the constant angular velocity (CAV) spindle motor control;
- avoid a long resynchronisation procedure when accessing a track that has been accessed before.

Previous reports on high-speed timing recovery used a customised analogue phase-locked loop [1, 2] or an all-digital phase-locked loop [3]. The former may require a long settling time and a resynchronisation interval whenever a new track is to be accessed, while the latter has limited frequency resolution due to its discrete-step control nature. In this paper, to achieve the aforementioned characteristics, a mixed-signal-controlled timing recovery circuit is proposed. The mixed-signal-controlled timing recovery circuit combines the characteristics of analogue phase-locked loops and all-digital phase-locked loops. Thus, it has several features, such as high frequency resolution, broad frequency range and fast acquisition.

For instance, in the CD-ROM system, the data are encoded in a series of pits and lands on a compact disc. When read by the laser pick-up head, the pits generate low voltage while the lands are represented by high voltage. The size of a pit, and conversely of a land, on optical discs is limited. In other words, transitions between lands and pits cannot occur too frequently or too infrequently. The transition frequency rule says that the run length of '0's or '1's must be no more than ten and no less than two. To comply with such a rule, the data to be recorded are first encoded using the eight-to-fourteen modulation (EFM) scheme. The EFM method translates an 8-bit data word from the original data stream into 14 channel bits using fixed mapping. Then three merging bits are inserted between two consecutive groups of 14 channel bits and a differential encoding scheme is applied. The relationship between the original data, encoded data signal, EFM data signal, and

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Y.-B. Luo is with the SoC Technology Center, Industrial Technology Research Institute, and was with National Taiwan University, Taipei 10617, Taiwan, Republic of China

T.-D. Chiueh is with the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan, Republic of China

Fig. 1 Example of eight-to-fourteen modulation signals

pit/land configuration is depicted in Fig. 1. The goal of the timing recovery circuit is to regenerate the transmitted clock from the channel EFM data signal and then sample the channel EFM data signal to recover the original data.

After timing recovery, the sampled data bits need be synchronised through a frame synchronisation circuit. This then sets up 14-bit blocks for further EFM demodulation. The demodulated 8-bit output data can be decoded by a channel error-correcting-code decoder and then sent for more signal processing or output to the host device.

2 Timing recovery circuit

The block diagram of the proposed mixed-signal-controlled timing recovery circuit is shown in Fig. 2. It consists of a mixed-signal-controlled oscillator (MSCO), a phase detector, a charge pump and a loop filter. The mixed-signal-controlled oscillator contains a voltage-to-current converter, a digital-to-current converter and a current-controlled oscillator. The voltage-to-current converter and the digital-to-current converter together supply the current to adjust the operating frequency of the current-controlled

Fig. 2 Mixed-signal-controlled timing recovery circuit

oscillator. By way of using a digital control word, the current-controlled oscillator can operate in a broad frequency range with fast switching speed. Within a small discrete frequency step, we utilise a charge-pump phase-locked loop to further fine-tune the oscillation frequency.

When the data on a CD or a DVD disc are to be read, the laser diode needs be moved to the corresponding track so the addressed data can be read out. If we use the CAV technique to control the spindle motor, the data recorded on different tracks have different data rates. To speed up the acquisition process, the proposed timing recovery circuit first reads in a digital frequency control word corresponding to the track location. In this way, the mixed-signal-controlled oscillator can acquire an approximate clock frequency and then the internal charge-pump phase-locked loop kicks in and locks on to a more accurate clock.

2.1 Mixed-signal-controlled oscillator

The core of the mixed-signal-controlled timing recovery circuit is an oscillator controlled by both digital and analogue signals. It includes the following three parts: a digital-to-current converter, a voltage-to-current converter and a current-controlled oscillator.

The digital-to-current converter converts the digital control word into an analogue current. With such a digital-to-analogue converter, changes in the control word directly reflects on the output current, thus switching the oscillation frequency swiftly. Figure 3 shows the circuit diagram of the digital-to-current converter. There are nine groups of current sources in the digital-to-current converter. Each group uses NMOS and PMOS devices as switches. When the Dx bit is high, the bias voltage is set to 'D2C bias'. Conversely, when Dx is low, the bias voltage is set to V_{dd} . The bias voltage controls several PMOS devices with binary-weighted widths which translate the binary control word into a current proportional to the value of the control word. The output current of the digital-to-current converter is of the form $y = mx + b$. The intercept value b is decided

Fig. 3 Circuit diagram of the digital-to-current converter

by the offset current in the digital-to-current converter. By adjusting the bias voltage of the offset stage, the lower limit of the output current can be controlled. The D2C bias regulates the slope m and thus the gain of the converter. The output current range of the digital-to-current converter is from I_{OFFSET} to $I_{OFFSET} + 255I_{LSB}$. SPICE simulation results show that the output current of the digital-to-current converter is proportional to the digital control word.

The analogue control circuit of the mixed-signal-controlled oscillator provides a small-scale current to enhance the frequency resolution. Since the oscillator control signal from the loop filter is a voltage signal, a voltage-to-current converter is required. Figure 4 shows the circuit diagram of the voltage-to-current converter. The transistor M is used as a voltage-controlled resistor. The control signal from the loop filter changes the output current of the voltage-to-current converter by adjusting the gate bias of transistor M. The left part of the voltage-to-current converter is similar to the digital-to-current converter except for a multiplexer, which controls the transconductance of the voltage-to-current converter.

The current-controlled oscillator generates a wide-frequency-range clock signal controlled by the currents supplied from the digital-to-current and the voltage-to-current converter. It includes three blocks: a bias generator, a differential-delay-cell-based ring oscillator and a differential-to-single-ended converter as shown in Fig. 5. The bias generator translates the input currents from the digital-to-current and the voltage-to-current converters to two bias

Fig. 4 Circuit diagram of the voltage-to-current converter

Fig. 5 Block diagram of the current-controlled oscillator

voltages, V_{ctrl} and V_{sc} . The two bias voltages adjust the delay time of the delay cells in the ring oscillator and so the oscillation frequency can be tuned. Because the output of the delay cell cannot reach full swing, a differential-to-single-ended converter is incorporated at the oscillator output. The ring oscillator is composed of three delay cells. Each delay cell consists of a differential pair with symmetric loads [4], shown in Fig. 6a. With differential signalling and symmetric load, the oscillator is almost immune from the noises coupled from the supply rail. Using a current mirror and a symmetric load, the bias generator, shown in Fig. 6b, produces two bias voltages for the delay cells V_{sc} and V_{ctrl} . A simple differential-to-single-ended converter is used to convert the output differential signal into a single ended signal.

2.2 New phase detector

The phase detector in a timing recovery application is a circuit used to measure the phase difference between the internal clock and the incoming data signal. Two NRZ-data

Fig. 6 Circuit diagrams
a Symmetric load differential delay cell
b Bias generator

phase detectors are proposed in [5] and [6], respectively. As mentioned in [6], the phase detector in [5] causes the VCO control voltage to drift precariously. Moreover, the phase detector proposed in [6] cannot operate in such a wide frequency range as in our application. Therefore, a phase detector is proposed.

Referring to Fig. 7a, the positive edge of the MSCO clock is to align with either positive or negative edges of the incoming EFM signal. In the first case, the MSCO clock leads the EFM signal. Signal $Q1'$ switches its state at the MSCO positive edge nearest the edge of the EFM signal. Signal $Q2'$ switches its state at the next positive edge of the MSCO clock. When the EFM and $Q2'$ signals are fed to an XOR gate, the $PDUP$ signal can be generated. Similarly, the $Q1'$ and $Q2'$ signals together generate the $PDDN$ signal. In the first case, the width of $PDDN$ pulse is wider than the $PDUP$ signal and so the MSCO clock slows down. However, if the MSCO clock lags the EFM signal, such as in the second case, the $PDUP$ pulse will be wider than the $PDDN$ pulse and so the MSCO clock will speed up.

We note that, owing to causality, the $Q1'$ signal cannot be directly generated. So we proposed to delay all signals by half a clock cycle, and the causality problem can be solved.

Fig. 7 Timing diagram of the proposed phase detector
a Original timing
b Revised timing

The revised timing diagram is shown in Fig. 7b. Note that the EFM signal is first delayed by half an MSCO clock period through a three-stage delay line identical to the one in the MSCO to get the signal A . In order to get the $Q1$ signal, the EFM signal is fed to the input of a negative edge-triggered D flip-flop clocked by the MSCO clock signal. Then $Q1$ is fed to another negative edge-triggered D flip-flop to produce the $Q2$ signal. $PDDN$ and $PDUP$ are generated according to

$$PDUP = (A \oplus Q2) \cdot Enable \quad (1)$$

$$PDDN = (Q1 \oplus Q2) \cdot Enable \quad (2)$$

where $Enable$ is a control signal that enables the phase detector. As a comparison, Fig. 8 illustrates waveforms of

Fig. 8 Comparison between a conventional phase detector (detector 1) and the proposed phase detector (detector 2)

Figure 9 depicts the circuit diagram of the proposed phase detector. The delay line consists of three delay cells which are identical to the delay cell used in the current-controlled oscillator and they are controlled by the same two bias voltages (V_{sc} and V_{ctrl}) generated from the MSCO. So, in principle, the delay of the delay line is approximately half a period of the MSCO clock. Furthermore, since the delay line is controlled by the two bias voltages from the MSCO in a master-slave fashion, the delay line delays the incoming signal by half a clock period regardless of possible temperature and process variations if the circuit is laid out carefully. However, the output of the delay cell is a differential signal, thus, a differential-to-single-ended converter is included at the end of the delay line. In order to properly align the three signals ($Q1$, $Q2$ and A), the outputs of the negative edge-triggered D-type flip-flops must also include the differential-to-single-ended converter. Simulation results of the proposed phase detector show that the delay line can provide an exact half-clock-cycle delay, so no static phase error occurs and the phase detector functions correctly.

The charge-pump circuit is used to translate the digital phase error signals *PDUP* and *PDDN* into current signals that charge or discharge the loop filter circuit. Figure 10

The frame synchronisation block, shown in Fig. 11, has several objectives. First, it detects the synchronisation pattern in a frame to acquire the correct frame timing. If it identifies a synchronisation pattern and another synchronisation pattern again after exactly 588 clock cycles (one frame length), frame synchronisation is completed. Secondly, the frame synchronisation block decomposes the frame stream into thirty-three channel words and removes the merging bits in between to prepare the 14-bit EFM data words for the eight-to-fourteen demodulation block. Thirdly, the frame synchronisation block generates several timing signals for the rest of the data recovery circuit, such as the clock of the input and output registers in the eight-to-fourteen demodulation circuit, synchronisation signal and subcode signal (active when the output data is the subcode). In addition, a test pattern generator is incorporated in the frame synchronisation block to test the function of the eight-to-fourteen demodulation block.

The eight-to-fourteen demodulator is implemented in a programmable logic array (PLA). We include an erasure flag to accommodate the situation that the input data does not belong to any of the 256 possible EFM codewords. In order to improve the speed of the PLA, a dynamic clocking scheme is adopted [8].

4 Experimental results

The proposed timing and data recovery chip for high-speed CD-ROM drives is fabricated through a 0.6µm n-well SPTM CMOS process. The photograph of the chip is illustrated in Fig. 12.

Fig. 12 Photograph of the timing and data recovery chip

In order to measure the characteristic of the mixed-signal-controlled oscillator, the charge-pump phase-locked loop is disabled so that the timing recovery circuit is an open loop. Figure 13 depicts the measured output frequency for

Fig. 13 Measured output frequency against digital control word at different bias voltages for mixed-signal controlled oscillator

various frequency control words and various bias voltages. There are four curves for different D2C bias voltages and offset bias voltages. The nonlinearity is caused by the current-controlled oscillator. However, each MSCO can be calibrated and a map between the frequency control word and the MSCO output frequency can be set up. Furthermore, the calibration process can determine appropriate values for the two parameters: D2C bias voltage and offset bias voltage, which then set the lowest output frequency and the gain of the digital portion of the MSCO.

The timing recovery is then tested with distorted random eight-to-fourteen modulated frame sequence of different clock rates. We measured the timing recovery circuit from 70 to 166.67 MHz. Figure 14 shows the measured eye patterns at 166.67 MHz and 70 MHz. The first waveform is the input data signal, i.e. the eight-to-fourteen modulated frame sequence with run length from three to eleven clock periods. The second waveform is the clock generated from the timing recovery circuit. The third waveform is the sampled and differentially decoded bit sequence. In both cases note how well the positive edges of the recovered clock

Fig. 14 Measured eye patterns at two different clock rates
a 166.67 MHz
b 70 MHz

signal align with the transitions of the input waveform. The first waveform has no extra transition inside three-clock-period intervals in both directions. Moreover, since the third waveform is the differentially decoded result of the first waveform, there exist at least two periods of '0' between two '1' pulses. The delay of one clock cycle between the input signal and the differentially decoded signal is due to a flip-flop after the differential decoder. Moreover, Fig. 15 shows the peak-to-peak jitter of recovered clock at 166.67 MHz and 70 MHz. We used the positive edge of the input data signal as the trigger signal to obtain the clock jitter. The peak-to-peak jitters are about 1.22 ns and 290 ps, respectively.

The advantage of using a mixed-signal-controlled oscillator in timing recovery can be evident in the following experiment. With the timing recovery circuit running stably at one clock frequency, we change the clock speed of the distorted incoming EFM signal and at the same time switch the digital control word of the MSCO to a precalculated value corresponding to the EFM signal frequency. Figure 16a shows the case of the EFM signal switching

Fig. 15 Measured peak-to-peak clock jitters at two different clock rates
a 166.67 MHz
b 70 MHz

Fig. 16 Measured output clock period during frequency switching
a 83.33 MHz to 166.67 MHz
b 166.67 to 83.33 MHz

from 83.33 MHz to 166.67 MHz, whereas Fig. 16b shows the case of switching from 166.67 MHz to 83.33 MHz. In both cases, the acquisition time is very short and is much less than 1 μ s under a loop bandwidth of 1 MHz. Normally, an analogue PLL will spend quite a long time before settling to the new clock frequency. However, in the proposed mixed-signal-controlled PLL scheme, due to the digital control nature of the MSCO, the timing recovery circuit can switch to the new frequency promptly. The experimental results obtained for the proposed chip are summarised in Table 1.

5 Conclusions

In this paper, the architecture and circuit design of a novel mixed-signal-controlled PLL-based timing recovery and data recovery chip have been described. Instead of an analogue PLL or an all-digital PLL, the proposed timing recovery circuit utilised a mixed-signal-controlled oscillator (MSCO) that combines both the advantages of analogue and digital PLLs, namely, high frequency, low jitter and fast switching. In order to accommodate NRZ data format in

Table 1: Chip summary

Technology	0.6 μm CMOS
Supply voltage	5 V
Working frequency	70–180 MHz
Switching time	< 1 μs
Power consumption (timing recovery)	85 mW
Power consumption (whole chip)	575 mW
Active area (timing recovery)	0.7 $\times$ 0.7 mm ²
Die area	2.8 $\times$ 2.8 mm ²

optical storage drives, a new phase detector was also proposed. These two components together with a charge-pump circuit and a loop filter constitute the proposed timing recovery circuit. A frame synchronisation detector, timing generation circuit and an EFM data demodulation circuit make up the data recovery circuit. The whole chip is fabricated in a 0.6- μm n-well SPTM CMOS process. The data recovery circuit has been tested to be functional at as high as 166.67 MHz. The timing recovery circuit achieves an operating frequency range of 70–180 MHz and its

acquisition time is much less than 1 μs while drawing only 85 mW from a 5 V power supply.

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