A 4–91-GHz Traveling-Wave Amplifier in a Standard 0.12-μm SOI CMOS Microprocessor Technology

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Abstract—This paper presents five-stage and seven-stage traveling-wave amplifiers (TWA) in a 0.12-μm SOI CMOS technology. The five-stage TWA has a 4–91-GHz bandpass frequency with a gain of 5 dB. The seven-stage TWA has a 5–86-GHz bandpass frequency with a gain of 9 dB. The seven-stage TWA has a measured 18-GHz noise figure, output 1-dB compression point, and output third-order intercept point of 5.5 dB, 10 dBm, and 15.5 dBm, respectively. The power consumption is 90 and 130 mW for the five-stage and seven-stage TWA, respectively, at a voltage power supply of 2.6 V. The chips occupy an area of less than 0.82 and 1 mm for the five-stage and seven-stage TWA, respectively.

Index Terms—Broadband CMOS circuit, CPW transmission line, high gain bandwidth product, SOI, traveling waveguide amplifier.

I. INTRODUCTION

TRAVELING-WAVE amplifier architecture (TWA) is widely used for broadband amplification in high-speed communication systems as well as for broadband radar applications. Several papers using state-of-the-art compound III-V technologies have reported frequency bandwidth as high as 50–100 GHz [1]–[3]. With the advance of deep-submicron CMOS technology, NFET devices with high $F_t$ and $F_{max}$ cut-off frequency are now available to the designer. However, despite recent progresses made by CMOS technology, the reported bandwidth for distributed amplifiers is still below 23 GHz [4]. These much lower performances achieved by bulk CMOS technology are due to the much higher parasitic capacitance of bulk silicon FETs as compared to III-V technologies. Another issue for silicon technologies is the losses in transmission lines like coplanar waveguide above the lossy silicon substrate. Silicon-on-insulator (SOI) CMOS is well known for its advantages for high-speed and low-power microprocessor applications [5]. SOI CMOS is also recently emerging as a possible candidate to expand CMOS to low-power millimeter-wave digital and RF applications [6], [13]. In this paper, we describe a five- and seven-stage broadband distributed amplifier fabricated in a SOI CMOS technology with a 3-dB cut-off frequency as high as 91 GHz.

Fig. 1. NFET current gain cut-off and transconductance versus gate length.

II. 0.12-μm SOI MICROPROCESSOR TECHNOLOGY

The TWA was designed in a 0.12-μm SOI CMOS microprocessor production technology without any process modification. This technology offers a low-parasitic NFET transistor with a measured peak $F_t$ in excess of 150 GHz for gate length smaller than 60 nm (Fig. 1). As shown in Fig. 1, with a measured NFET transconductance of more than 1-mS/μm, this technology is comparable to state-of-the-art GaAs FET. In order to achieve the highest $F_{max}$ possible, the multifinger FET layout must be optimized. A $F_{max}$ in excess of 200-GHz was measured for a width of 2 μm per finger, as well as a minimum noise figure of less than 2 dB up to 26 GHz [14]. The technology also offers a hierarchical eight copper metal-layers in a FTEOS dielectric, a poly-resistor, and a MOS capacitor.

One of the main challenges with digital silicon technology is the integration and modeling of the transmission line and a linear capacitor on lossy Si substrate. Microstrip lines, with ground plane on the first layer of metal and signal on the last layer of metal can be used. However, since the last layer of Cu metal is only 9.8-μm from the Si substrate, the integration of
low-losses 50-Ω microstrips is difficult. In the coplanar waveguide (CPW) configuration, the distance between the ground planes and the signal line is a free parameter (Fig. 2). The drawback of CPW is that the signal is not any more shielded from the substrate, and if the signal line is too wide, substrate losses are high. Fig. 2 shows a simplified equivalent circuit used to model the CPW line on SOI. This model includes the inductor line, its associated resistor to model the ohmic losses, the capacitive coupling to the substrate and to the ground planes, as well as the substrate high-pass RC network. Beyond the frequency relaxation of the substrate, which is 10 GHz for the 15-Ω·cm substrate used to fabricate the circuit, the substrate resistor is shorted by the substrate capacitor, and the CPW behaves more like a regular CPW on insulator substrate.

The CPWs were implemented on the last 1.2-μm-thick metal layers to reduce the parasitic capacitance to the substrate. Since no MIM capacitors are available in a digital process, we integrated a linear capacitor in a standard microprocessor by designing a 3-D vertical parallel plate capacitor [15]. We measured a record density of 1.8-fF/μm² in an eight layers of metal FTOES BEOL for the vertical native capacitor, with Q higher than 100 at 1 GHz for a 1.1-pF capacitor and a resonant frequency of 10 GHz.

III. 4–90-GHz CPW SOI DISTRIBUTED AMPLIFIER DESIGN

Fig. 3 shows a circuit schematic of the n-stage distributed amplifier. The circuit is based on cascode cells \((Q_{1a}, Q_{1b})\) that allow good isolation and high cut-off frequency. Each amplifier cell is part of an input and output transmission line. The input cascode-cell capacitor, mainly \(Q_{1a}C_{gs}\), contributes to the input transmission line impedance. The output cascode-cell capacitor, mainly \(Q_{1b}C_{ds}\), contributes to the output transmission line impedance. Therefore, the transmission lines were synthesized taking into account \(Q_{1a}C_{gs}\) and \(Q_{1b}C_{ds}\) to achieve 50-Ω matching. Usually, RF S-parameters taken on a transistor provide accurate data for the TWA design. In this design, we took advantage of the scalable FET model to optimize the width of \(Q_{1a}\) and \(Q_{1b}\), so that \(Q_{1a}C_{gs}\) and \(Q_{1b}C_{ds}\) are equal. This allows, unlike previously reported implementations, to achieve a compact, simple and perfectly symmetrical layout. The cascode transistors are biased through the bias resistor \(R_n\). A bypass capacitor \(C_n\) is used to avoid, to draw current in the 50-Ω input and output matching resistors. However, \(C_n\) capacitors give a bandpass structure to the amplifier. In theory, \(C_n\) can be chosen arbitrarily high to satisfy any low-frequency system requirement. Practically, the \(C_n\) size is limited by its resonant frequency. This was a great concern for the design, because there was limited data available beyond 40 GHz for passive components. The \(Q_{1a}\) gate and \(Q_{1b}\) drain are biased through the Vectorial Network S-parameters Analyzer bias-tee. The ground metal islands in between amplifier stages are connected to the peripheral metal ground through metal strips. The eight metal layers were fully used to simplify the layout and reduce the overlap parasitic capacitors between metal lines.

IV. MEASURED RESULTS

All the measurements were done on wafer using a 110-GHz Vectorial Network analyzer. The five- and seven-stage distributed amplifiers were measured at a biasing current of 35 and 51 mA, respectively, and \(V_{dd} = 2.6\) V. Fig. 4 shows the measured gain S21 up to 110 GHz. A gain of 5 and 9 dB is achieved with a 3-dB cut-off frequency of 91 and 86 GHz for the five- and three-stage amplifiers, respectively. A state-of-the-art 0.18-μm bulk CMOS TWA reported in [4] is shown as a reference (Fig. 4). Below 4 GHz, the gain increases because of the small bypass capacitor used. The low-frequency cut-off can be decreased by using a larger decoupling capacitor or by using some active matching techniques.

Fig. 5 shows the input reflection coefficient up to 110 GHz. The input matching is better than −7 dB from 4 GHz up to 110 GHz. Below 4 GHz, the amplifier is not well matched because of the size of the bypass capacitor \(C_n\) used. Once plotted on a Smith chart (Fig. 6), the input reflection coefficient, behaves as expected as a spiral, because of increasing CPW transmission losses with frequency. The output reflection coefficient exhibits the same behavior as for the input. The spiral centers is slightly offset from the 50-Ω Smith-chart center, due to an underestimation of the line capacitor by our models, shifting the CPW line impedance to a lower impedance than 50 Ω. The output matching is better than −7 dB from 4 GHz up to 90 GHz. Fig. 7 shows the measured isolation up to 110 GHz. The isolation is better than 15 and 20 dB up to 110 and 60 GHz for both TWAs, respectively. The isolation is surprisingly good for Si technology in the 100-GHz regime. All these measurements demonstrate that, if carefully designed, the 3-D vertical parallel plate capacitor and the CPW on SOI are low-loss, very broadband, and do not exhibit parasitic resonant frequencies up to 110 GHz. It also demonstrates that the input and output pads on lossy Si substrate can be designed to properly launch electromagnetic waves up to 90 GHz. All the measurement data include the effects of the input and output RF pads. In other words, the input and output pads were not calibrated out. The input and output RF pads seem not to degrade the performance of the TWA even up to 100 GHz, because the pads are part of the CPW transmission lines. Fig. 8 shows the output power versus input power measured at 20 GHz for the seven-stage TWA. A 10-dBm output 1-dB compression point is measured at 20 GHz. This demonstrates that significant output power can also be generated by Si technology at millimeter-wave frequency. Some measurements were also done at 50 GHz, but because of the increased cable losses and frequency synthesizer output power drop beyond 20
GHz, we were not able to compress the TWA at that frequency. As shown in Fig. 9, at 50 GHz the third-order output IP3 is 16 and 15.5 dBm for the five- and seven-stage TWAs, respectively. We did some other IP3 measurements at 20 GHz, and we measured a 10.5- and 15-dBm output IP3 for the five- and seven-stage TWA, respectively. The 20-GHz output IP3 for the five-stage TWA is much lower for some reasons we do not yet understand. Noise measurements were taken between 10 and 18 GHz on 50 Ω, as shown in Fig. 10, with an Agilent 8971 C down-converter and 8970 B noise figure meter. A 5.5-dB noise figure...
V. STATE-OF-THE-ART DISTRIBUTED AMPLIFIER DESIGN COMPARISON

Table I compares several distributed amplifiers designed in different technologies for gain, matching, bandwidth, and area. The 0.12-μm SOI TWA exhibits four times higher 3-dB cut-off frequency than previously reported state-of-the-art 0.18-μm bulk RF CMOS technology. For the first time a CMOS technology can offer gain, bandwidth, and power performances comparable to state-of-the-art compound III-V technologies. The improvement in gain and bandwidth highlight the low-parasitic and high-\(F_{\text{max}}\) advantages of SOI technology over bulk technology. A quality factor for the SOI NFET-based TWA can be defined as the ratio of the 3-dB cut-off frequency of the TWA to the current gain cut-off frequency. In our case, this factor is about 60%, which is slightly lower than the one reported by mature III-V technologies [2], which is 70%. The gain-bandwidth product (GBW) is 161 and 242 GHz for the five- and seven-stage TWA, respectively. Table II compares noise figure, linearity, and power consumption. The noise performance is comparable to other state-of-the-art TWA.

### Table I

<table>
<thead>
<tr>
<th>Technology</th>
<th>S21 (dB)</th>
<th>S11/S22 (dB)</th>
<th>Bandwidth (GHz)</th>
<th>Area (mm²)</th>
</tr>
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<tr>
<td>0.18-μm bulk CMOS</td>
<td>7.3 ± 0.8</td>
<td>&lt; -8 / &lt; -9</td>
<td>0.6 - 22</td>
<td>0.90 X 1.50</td>
</tr>
<tr>
<td>InAlAs HBT</td>
<td>5.1 ± 1.2</td>
<td>&lt; -5 / &lt; -5</td>
<td>2.0 - 50</td>
<td>1.80 X 1.20</td>
</tr>
<tr>
<td>InP HEMT</td>
<td>14 ± 0.8</td>
<td>&lt; -9 / &lt; -10</td>
<td>1.0 - 90</td>
<td>2.50 X 1.10</td>
</tr>
<tr>
<td>GaAs HEMT</td>
<td>6.0 ± 1.0</td>
<td>&lt; -13 / &lt; -4</td>
<td>2.0 - 50</td>
<td>1.97 X 1.25</td>
</tr>
<tr>
<td>SOI-7stg</td>
<td>7.8 ± 1.3</td>
<td>&lt; -7 / &lt; -7</td>
<td>4.0 - 86</td>
<td>1.46 X 0.72</td>
</tr>
<tr>
<td>SOI-5stg</td>
<td>4.0 ± 1.2</td>
<td>&lt; -7 / &lt; -7</td>
<td>4.0 - 91</td>
<td>1.11 X 0.72</td>
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</table>

### Table II

<table>
<thead>
<tr>
<th>Technology</th>
<th>N.F. (dB)</th>
<th>OP1dB (dBm)</th>
<th>OIP3 (dBm)</th>
<th>Vdd (V)</th>
<th>PDC (mW)</th>
<th>Ref</th>
</tr>
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<td>0.18-μm bulk CMOS</td>
<td>4.3-6.1</td>
<td>-</td>
<td>-</td>
<td>1.3</td>
<td>52</td>
<td>[4]</td>
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<tr>
<td>InAlAs HBT</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>4</td>
<td>89</td>
<td>[1]</td>
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<tr>
<td>InP HEMT</td>
<td>8.0 - 9.0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>[2]</td>
</tr>
<tr>
<td>GaAs HEMT</td>
<td>-</td>
<td>22</td>
<td>-</td>
<td>15</td>
<td>1900</td>
<td>[3]</td>
</tr>
<tr>
<td>SOI-7stg</td>
<td>5.0 - 3.6</td>
<td>10</td>
<td>15.5</td>
<td>2.6</td>
<td>130</td>
<td>This work</td>
</tr>
<tr>
<td>SOI-5stg</td>
<td>6.2 - 4.2</td>
<td>9</td>
<td>16</td>
<td>2.6</td>
<td>90</td>
<td>This work</td>
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Fig. 8. Measured 1-dB compression point for the seven-stage TWA.

Fig. 9. Third-order IMD measurements at 50 GHz.
power, for Si technology, generated at millimeter frequency. The actual chip areas are less than 0.82 and 1 mm² for the five-stage and seven-stage TWA, respectively. These results demonstrate that broadband and low-losses pads and passives can be integrated in a standard SiO technology. It also demonstrates, with such a fundamental amplification function, the low-parasitic advantage of SiO over bulk CMOS technology and its potential for the design of millimeter-wave ultra-high-speed and broadband monolithic-microwave integrated circuits.

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REFERENCES

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Jean-Olivier Plouchart (M’96) was born in Paris, France in 1966. He received the M.S. and the Ph.D. (Hon.) degrees in electrical engineering from Paris VI University, France, in 1988 and 1994, respectively. During his masters work, he spent ten months working at Alcatel Telspace on the design of MESFET GaAs MMICs for satellite telecommunications.

From 1989 to 1990, he was a Scientist Consultant at the ETCA as part of his military service. From 1990 to 1994, he was with the French Telecom Laboratory (CNET), as a Ph.D. student, working to develop the GaAs HBT technological process and to design HBT MMICs for DCS1800 wireless and high bit rate optical communications. In 1994, he joined the University of Michigan as a Research Fellow, where he designed high-speed circuits using a 100-GHz InP HBT process. In 1996, he joined the IBM T. J. Watson Research Center as a Research Scientist, where his work involved the design of SiGe BiCMOS and CMOS RFIC circuits for wireless LAN applications. In 2000, he led a team working on low-power high-performance SOI SoC technology, and pioneered the design of millimeter wave SOI CMOS in standard microprocessor technology. His research interests include solid-state technologies, the design and optimization of high-speed circuits, the integration of RF transceivers with microprocessors for SoC applications, and the design automation of SoC design. Currently, he manages the development of high-speed design and technology benchmarking at the IBM Microelectronics Semiconductor Research and Development Center. He holds two patents, and has authored or coauthored over 45 publications.

Dr. Plouchart was a coauthor of the paper that won the Best Student Paper Award at the 2002 IEEE Radio Frequency Integrated Circuit Conference.

Jonghe Kim (S’98–M’01) was born in Incheon, Korea, in 1961. He received the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, in 2001.

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Jean-Olivier Plouchart was a Scientist Consultant at the ETCA as part of his military service. From 1990 to 1994, he was with the French Telecom Laboratory (CNET), as a Ph.D. student, working to develop the GaAs HBT technological process and to design HBT MMICs for DCS1800 wireless and high bit rate optical communications. In 1994, he joined the University of Michigan as a Research Fellow, where he designed high-speed circuits using a 100-GHz InP HBT process. In 1996, he joined the IBM T. J. Watson Research Center as a Research Scientist, where his work involved the design of SiGe BiCMOS and CMOS RFIC circuits for wireless LAN applications. In 2000, he led a team working on low-power high-performance SOI SoC technology, and pioneered the design of millimeter wave SOI CMOS in standard microprocessor technology. His research interests include solid-state technologies, the design and optimization of high-speed circuits, the integration of RF transceivers with microprocessors for SoC applications, and the design automation of SoC design. Currently, he manages the development of high-speed design and technology benchmarking at the IBM Microelectronics Semiconductor Research and Development Center. He holds two patents, and has authored or coauthored over 45 publications.

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