A 5-GHz Low Phase Noise Differential Colpitts CMOS VCO

Ming-Da Tsai, Student Member, IEEE, Yi-Hsien Cho, and Huei Wang, Senior Member, IEEE

Abstract—A low noise 5-GHz differential Colpitts CMOS voltage-controlled oscillator (VCO) is proposed in this letter. The Colpitts VCO core adopts only PMOS in a 0.18-µm CMOS technology to achieve a better phase noise performance since PMOS has lower 1/f noise than NMOS. The VCO operates from 4.61 to 5 GHz with 8.3% tuning range. The measured phase noise at 1-MHz offset is −120.42 dBc/Hz at 5 GHz and −120.99 dBc/Hz at 4.61 GHz. The power consumption of the VCO core is only 3 mW.

To the authors’ knowledge, this differential Colpitts CMOS VCO achieves the best figure of merit (FOM) of 189.6 dB at 5-GHz band.

Index Terms—Analog integrated circuits, CMOS integrated circuits, low phase noise, RFIC, voltage-controlled oscillators (VCOs), wireless local area network (WLAN).

I. INTRODUCTION

FULLY-INTEGRATED voltage-controlled oscillators (VCOs) are important building blocks in the implementation of a single radio chip in today’s communication systems. Recently, the increasing demand for high speed data communication drives us to 5-GHz band rather than 2.4-GHz band for wireless LAN application, such as IEEE802.11a and HIPERLAN, where 5-GHz band is used, can enable the high communication drives us to 5-GHz band rather than 2.4-GHz systems. Recently, the increasing demand for high speed data transmission of up to 54 Mbps.

Recently, many 2.4- and 5-GHz VCOs have been published [1]–[7]. The most popular topology of voltage-controlled oscillator is cross-coupled structure due to its easy design and start-up oscillation condition. Using SiGe technology, two 5-GHz VCOs were also presented in [1] and [2], respectively. A 5-GHz complementary VCO with good figure of merit (FOM) was published in [3], realized using 0.13-µm SOI CMOS process. Low noise 5-GHz InGaP/GaAs HBT VCOs were demonstrated in [7] with the best result among the reported compound semiconductor FET and HBT VCOs. In order to reduce phase noise contributed from cross-coupled transistors, a 2.4-GHz PMOS cross-coupled VCO fabricated by 0.18-µm CMOS technology was reported, with a phase-noise improvement of 15 dB compared with NMOS cross-coupled VCO[17]. For the same reason, 5-GHz PMOS cross-coupled VCOs were demonstrated in [4], [6] and 2.4-GHz VCO with PMOS cross-coupled structure and selective metal parallel shunting inductor in [12].

Besides cross-coupled structures, Colpitts oscillator is also a good choice for implementation of low noise CMOS VCO [13]. A 1.8-GHz differential NMOS Colpitts VCO was demonstrated in [8] with phase noise of −138.2 dBc/Hz at 3-MHz offset.

In this letter, we demonstrated a 5-GHz CMOS VCO based on Colpitts topology in 0.18-µm CMOS technology. In order to reduce the flicker noise upconversion, this core of differential Colpitts VCO is realized using PMOS transistors except of the output buffer. The measurements results show that the VCO operates form 4.6 to 5 GHz with 8.3% tuning range, and phase noise of −120.42 dBc/Hz at 1-MHz offset. The power consumption of the VCO core is only 3 mW and the output power is higher than 1 dBm. To the author’s knowledge, this differential Colpitts CMOS VCO achieves the best FOM of 189.6 dB at 5-GHz band [10], [11].

II. VCO DESIGN AND IMPLEMENTATION

The flicker noise of a transistor is the cause of the close-in phase noise near the carrier in 1/f^3 region. In the CMOS process, the transistor 1/f noise is generally high and causes serious degradation of VCO phase noise performance. However, the 1/f noise of PMOS is usually lower than NMOS in one order of magnitude. In addition, the hot carrier effect in a PMOS transistor is typically smaller, which is especially important in a deep submicrometer CMOS process where hot electron noise (white noise) is significant [4]. The measured minimum noise figure (N_{Fmin}) of NMOS and PMOS transistors under the similar bias level also shows PMOS has lower N_{Fmin} than that of the NMOS [17]. Thus utilization of only PMOS transistors in the VCO core should reduce the phase noise in the 1/f^3 region, which is from 1/f noise, as well as the phase in the 1/f^2 region, which is mainly from the device white noise. Furthermore, the output buffers are NMOS and loaded through a capacitive divider consisting of C_1 and C_2. Thus, the loaded tank Q is larger than directly located across tank.

The differential Colpitts VCO can be realized by coupling two identical single-ended Colpitts VCO with odd mode oscillation and suppression of even mode oscillation. The circuit schematic is shown in Fig. 1. The common node of the identical oscillator is virtual ground at odd mode and open at even mode. Single-ended Colpitts VCO could use common-gate transistor and feedback capacitor to provide negative conductance and achieve the desired oscillation frequency. The gate of common-gate transistor needs to be bypassed by large enough capacitor. However, the large capacitor can be removed since virtual...
ground at common gate can be performed at odd mode operation. The even mode operation can also be suppressed by the bias resistor \( R_g \) at common gate since the large resistor can degrade the gain of the transistor.

The chip is fabricated in TSMC’s 0.18-\( \mu \)m MS/RF technology [19], [20], with a 2-\( \mu \)m AlCu top metal layer. The substrate conductivity is approximately 10 S/m. This technology can provide a \( f_T \) and \( f_{max} \) of better than 60 and 55 GHz, respectively. Fig. 2 shows the chip photograph with size of 550\( \times \)750 \( \mu \)m\(^2\) including dc and RF testing pads.

III. EXPERIMENTAL RESULTS

The measurement is performed on an FR-4 PCB. The VCO chip is mounted on the test board and connected to the output FR-4 grounded CPW line (\( Z_0 \approx 50 \Omega \)) by gold bond wires. Effects of bond wire and the FR-4 test board were all taken into account in simulation. The VCO core and buffer amplifier dissipate 3 and 6 mW, respectively. The measured oscillation frequency covers from 4.6 to 5 GHz with control voltage from -1.4 to 1 V, as shown in Fig. 3. The frequency control is achieved by the accumulation mode varactors. As shown in Fig. 4, the measured output power is better than 1 dBm at single port with 50-\( \Omega \) termination at the other port, which indicates the differential output power is better than 4 dBm. This CMOS VCO achieves dc-to-RF conversion efficiency of better than 28% over all tuning frequency. It is calculated by the ratio of differential output power and total power consumption of 9 mW. The measured phase noise, as shown in Fig. 5, is -120.42 dBC/Hz at 1 MHz offset at 5 GHz. The above free running measurement of the phase noise performance shows that the fully integrated CMOS VCO is sufficient for wireless communication applications. When the VCO is utilized in 5-GHz frequency synthesizer application, the phase noise can be further suppressed by the loop filter of PLL frequency synthesizer [14]–[16].
To compare the performance of previously published oscillators, figure of merit (FOM) is used as defined by [9]

$$FOM(dB) = 10 \log \left( \frac{(f_0)^2}{f_m} \cdot \frac{1}{P_n} \right).$$  \hspace{1cm} (1)

Table I summarizes measurement results and the previously reported 5-GHz VCOs. The phase noise (PN) is measured at 1-MHz offset.

<table>
<thead>
<tr>
<th>Process</th>
<th>Freq. (GHz)</th>
<th>Vdd (V)</th>
<th>Core $P_{dd}$ (mW)</th>
<th>PN (dBc/Hz)</th>
<th>FOM</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25μm SiGe BICMOS</td>
<td>4.4</td>
<td>2.7</td>
<td>21.6</td>
<td>-119</td>
<td>178.5</td>
<td>[1]</td>
</tr>
<tr>
<td>SiGe HBT</td>
<td>5.5</td>
<td>1.8</td>
<td>5</td>
<td>-116</td>
<td>183.8</td>
<td>[2]</td>
</tr>
<tr>
<td>0.13μm SOI CMOS</td>
<td>5.6</td>
<td>1</td>
<td>2</td>
<td>-114.6</td>
<td>186.6</td>
<td>[3]</td>
</tr>
<tr>
<td>0.25μm CMOS</td>
<td>5.35</td>
<td>1.5</td>
<td>7</td>
<td>-117</td>
<td>183.1</td>
<td>[4]</td>
</tr>
<tr>
<td>0.18μm CMOS</td>
<td>5.8</td>
<td>1.8</td>
<td>8.1</td>
<td>-110</td>
<td>176.2</td>
<td>[5]</td>
</tr>
<tr>
<td>GaAs HBT</td>
<td>4.39</td>
<td>3.5</td>
<td>14</td>
<td>-117.8</td>
<td>179.6</td>
<td>[6]</td>
</tr>
<tr>
<td>0.24μm CMOS</td>
<td>5.8</td>
<td>2.5</td>
<td>5</td>
<td>-112</td>
<td>180.3</td>
<td>[7]</td>
</tr>
<tr>
<td>0.25μm CMOS</td>
<td>5</td>
<td>2.5</td>
<td>13.75</td>
<td>-114</td>
<td>176.8</td>
<td>[8]</td>
</tr>
<tr>
<td>0.18μm CMOS</td>
<td>5</td>
<td>1.5</td>
<td>3</td>
<td>-120.42</td>
<td>189.6</td>
<td>This Work</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

In this letter, we demonstrated a 5-GHz CMOS VCO based on Colpitts topology in 0.18-μm CMOS technology. In order to reduce the flicker noise upconversion, this core of differential Colpitts VCO is realized using PMOS transistors. The VCO operates from 4.6 to 5 GHz with 8.3% tuning range, and phase noise of $-120.42$ dBc/Hz at 1 MHz offset. The power consumption of the VCO core is only 3 mW and the output power is higher than 1 dBm. To the author’s knowledge, this differential Colpitts CMOS VCO achieves the best FOM of 189.6 dB at 5-GHz band and efficiency ($P_{out}/P_{DC}$) of better than 28% over full tuning frequency.

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REFERENCES