A 6-bit 800-MS/s Pipelined A/D Converter With Open-Loop Amplifiers

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Abstract—A 6-bit 800-MS/s pipelined A/D converter (ADC) achieves SNDR and SFDR of 33.7 dB and 47.5 dB, respectively. Employing voltage-mode open-loop amplifiers in gain stages, global gain control techniques, and two-bank-interleaved architecture, the proposed pipelined A/D converter relaxes stringent design tradeoffs between speed and power. Fabricated in a 0.18- μm CMOS technology, the ADC consumes 105 mW from a 1.8-V power supply while the active area is only 0.5 mm².

Index Terms—Analog-digital conversion, CMOS analog integrated circuits, gain control.

I. INTRODUCTION

STATE-OF-THE-ART read channels in high-performance serial-link systems such as DVD disk drives and communication networks require high-speed ADCs to digitize the partial response signal for digital processing [1]. High-speed, low-resolution ADCs are dominated by flash architecture [2], [3]. Employing digital-circuit-like comparators, flash ADCs achieve high-speed conversion rates for a given technology but at the cost of higher power consumption. Pipelined ADCs can meet the needs of applications requiring medium-speed conversion rates, while improving power efficiency. One salient advantage of a pipelined ADC over a flash architecture is its low input capacitance, thereby relaxing the design requirement of preceding stage. The conversion speed of the conventional pipelined ADC architecture is limited by the need for high-gain and wide-bandwidth closed-loop amplifiers in the gain stages. Moreover, decreasing supply voltages in deep-submicron technologies restrain the design methodology of conventional high-gain amplifiers, such as cascode opamps. To overcome these barriers, several ADC designs applying open-loop amplifiers with digital calibration have been developed. In [4], an efficient method reduces the power consumption by replacing a closed-loop amplifier with an open-loop amplifier in the first stage of the pipelined ADC. References [5] and [6] use an ADC array to achieve GSample/s with current-mode open-loop amplifiers in pipelined stages.

To obtain high-speed conversion, time-interleaved techniques are prevalent in ADC designs. A time-interleaved ADC based

Fig. 1. System architecture.

on SAR architecture that achieves high speed and low power consumption has been presented in [7]. Pipelined ADCs with time-interleaved techniques [5], [6] can deliver even higher conversion performance than SAR ADCs [7].

In this work, a 6-bit pipelined ADC with open-loop amplifiers and a two-bank-interleaved technique are coupled to achieve the 800-Msample/s conversion rate in a 0.18- μm CMOS technology. Voltage-mode open-loop amplifiers enable the converter with pipelined architecture to operate at a higher conversion rate. Without the need of digital calibration, the global gain control technique compensates the gain attenuation in open-loop amplification due to parasitic capacitances. By using the interleaved technique, this ADC achieves high-speed operation with a reasonable power level. Note that it is not beneficial to apply the stage scaling technique in the proposed ADC to improve the efficiency at the 6-bit level.

Section II introduces the system architecture of the pipelined ADC with open-loop amplifiers. In Section III, the building blocks of the ADC are described. Section IV specifies the design considerations of this ADC. Experimental results are presented in Section V, and Section VI summarizes with a conclusion.

II. SYSTEM ARCHITECTURE

The pipelined ADC requires two nonoverlapped clocks to operate in different phases. The amplifier is in amplification mode for half of the cycle and in reset state for the other half. Shown in Fig. 1, two interleaved banks of pipelined ADC in different phases convert the sampled signal to digital data. Then, each bank of the ADC operates at 400 MHz and the entire ADC

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Fig. 2. (a) Closed-loop amplifier model. (b) Open-loop amplifier model.

achieves 800 Msample/s throughput, thereby relaxing the stringent bandwidth requirements of analog circuits. The track-and-hold amplifier (THA) is designed for better than 8-bit linearity. The pipelined ADC chooses four 1.5-bit stages to tolerate larger comparator offset voltage. A 2-bit flash ADC is cascaded at the end of pipelined stages to construct a 6-bit pipelined ADC. With delay alignment and error correction, the ADC produces digital code at the rate of 800 Msample/s. The servo loop of the global gain control ensures gain accuracy of pipelined stages. The interleaved ADC output is decimated by 21 for data processing.

In a conventional 6-bit pipelined A/D converter design, the open-loop gain of the amplifiers in the 1.5-bit stages must be greater than 40 dB. High-gain amplifiers require stringent design tradeoffs between power and settling time. In this work, open-loop amplifiers replace the conventional closed-loop amplifiers to achieve high-speed conversion with lower power.

Design tradeoffs between speed and power for closed-loop amplifiers and open-loop amplifiers are distinct. For a large input, the settling time of the closed-loop amplifier, an operational transconductance amplifier (OTA), may suffer from slewing at the initial time. To simplify the operation of closed-loop amplification, the model of the single-stage OTA is shown in Fig. 2(a). The transconductance of the OTA is g_m and the maximum output current is limited to $\pm I_{SS}$. The output transient response is obtained as (1) [8] for the output of the OTA changing from 0 to V_{ref} :

$$V_{out}(t) = V_{ref} + [V_{out}(t_{slew}) - V_{ref}] \cdot e^{-(t-t_{slew})/\tau} \quad (1)$$

where

$$\begin{aligned} V_{out}(t_{slew}) &= \frac{I_{SS}}{C_{LC} + C_F \parallel (C_S + C_P)} \cdot t_{slew} \\ t_{slew} &= \frac{\left(V_{ini} - \frac{I_{SS}}{g_m}\right) \cdot (C_{LC} + C_F \parallel (C_S + C_P))}{I_{SS}} \\ &\quad \cdot \frac{C_S + C_P + C_F}{C_F} \\ \tau &= \frac{(C_{LC} + C_F \parallel (C_S + C_P))}{g_m} \cdot \frac{C_S + C_P + C_F}{C_F} \end{aligned}$$

where V_{ini} is the initial condition of V_X , and t_{slew} is the slewing time of the OTA. When maximum output voltage is V_{ref} , the

response of total available time (t_{cav1}) for the following N -bit quantizer must satisfy

$$V_{out}(t_{cav1}) = V_{ref} - \frac{2V_{ref}}{2^{N+1}}. \quad (2)$$

Equation (1) and (2) lead to

$$t_{cav1} = t_{slew} + \tau \cdot \ln \frac{V_{ref} - V_{out}(t_{slew})}{(V_{ref}/2^N)}. \quad (3)$$

The open-loop amplifier is modeled in Fig. 2(b). Because the open-loop amplifier always operates at the linear amplification region, slewing does not occur. When the output of the open-loop amplifier changes from 0 to V_{ref} , the output voltage is obtained as

$$V_{out}(t) = V_{ref}(1 - e^{-t/\tau}) \quad (4)$$

where

$$\tau = R_L \cdot C_{LO}.$$

Similarly, the total available time of the open-loop amplifier is

$$t_{oav1} = \tau \cdot \ln 2^N. \quad (5)$$

For the typical design of amplifiers, $I_{SS} = 1$ mA, $C_S = C_F = 300$ fF, $C_{LC} = 600$ fF, $C_P = 100$ fF, $V_{ini} = 100$ mV, $g_m = 11$ mA/V, $V_{ref} = 200$ mV, and $N = 5$, the available time of the closed-loop amplifier, t_{cav1} , is equal to 0.57 ns. At the same power level, when $R_L = 500 \Omega$ and $C_{LO} = 300$ fF, the available time of the open-loop amplifier, t_{oav1} , is equal to 0.52 ns. Increasing I_{SS} or enlarging g_m in the closed-loop amplifier reduces t_{slew} but at the cost of higher power or larger parasitic capacitances and area. Moreover, stability problems arising from higher order poles must be carefully designed to avoid long settling time. Such tradeoffs present challenges in the design of high-performance amplifiers. Equation (4) indicates that the settling time of the open-loop amplifier is only the function of R_L and C_{LO} . Altering these parameters to enhance the operation speed is more efficient than those in closed-loop amplifiers. Additionally, the immunity from stability consideration relaxes tradeoffs between speed and power in the open-loop amplifiers. Consequently, the simple open-loop amplifier proves

Fig. 3. Track-and-hold circuit.

a better power-efficiency circuit than the complex closed-loop amplifier in the design of pipelined ADCs [4].

III. CIRCUIT DETAILS

A. Track-and-Hold Amplifier

The high-speed THA reduces the errors of clock skew and enhances the conversion rate preceding the first-stage comparators. Shown in Fig. 3, to reduce input-dependent turn-on resistance, the track-and-hold circuit adopts complementary MOS switches. Two dummy switches, M_3 and M_4 , with half size of M_1 and M_2 , absorb the input-dependent charge injection. CMOS switches and capacitors (C_H) sample the input signal. Then, nMOS source followers act as unity-gain buffers. The sources of M_5 – M_8 are tied to their own bulks by the deep-N-well process to eliminate body effect and reduce the threshold voltage. To obtain better matching and reduce clock feedthrough, C_H is conservatively chosen as 300 fF. Two interleaved THAs controlled by nonoverlapped clocks, ϕ_1 and ϕ_2 , sample the input signal for each bank of the pipelined stages.

B. Pipelined Stage With Open-Loop Amplifiers

The conventional flip-around radix-2 1.5-bit pipelined stage using a closed-loop amplifier is shown in Fig. 4(a). The multiplying DAC (MDAC) consists of a high-gain amplifier and capacitors, C_F and C_S . When clock ϕ_1 is high, S_{1a} , S_{1b} , S_{1c} are ON and S_{2a} , S_{2b} are OFF, V_i is sampled to C_F and C_S . The redundant-signed-digit (RSD) [9] code, D_i , which belongs to $[-1, 0, +1]$, is evaluated by comparing V_i with $V_{REF}/4$ and

$-V_{REF}/4$. When clock ϕ_2 is high, S_{1a} , S_{1b} , S_{1c} are OFF and S_{2a} , S_{2b} are ON, the output V_{i+1} is given by

$$V_{i+1} = \frac{1}{1 + \frac{1}{A_v} \cdot \frac{C_S + C_F}{C_F}} \times \left(\frac{C_S + C_F}{C_F} \times V_i - V_{REF} \cdot \frac{C_S}{C_F} \times D_i \right) \quad (6)$$

where A_v is the open-loop gain of the amplifier. For the case with $A_v = \infty$ and $C_F = C_S$, (6) is reduced to

$$V_{i+1} = 2 \times V_i - V_{REF} \times D_i. \quad (7)$$

Shown in Fig. 4(b), the gain of the open-loop amplifier needs to be 2 to scale up the difference between V_i and reference voltage. The operation of the pipelined stage with an ideal open-loop amplifier can be expressed as

$$V_{i+1} = 2 \times \left(V_i - \frac{V_{REF}}{2} \times D_i \right) \quad (8)$$

which is identical to (7). When clock ϕ_1 is high, S_{1a} , S_{1b} are ON and S_2 is OFF, input voltage V_i is sampled at node N . When clock ϕ_2 is high, S_{1a} , S_{1b} are OFF and S_2 is ON, node N is now connected to $V_{REF}/2$ to perform the operation of (8). Fig. 4(c) shows the implementation of the differential open-loop pipelined stage, where only upper half switches and capacitor network are illustrated for simplicity. When clock ϕ_1 is high, S_{1a} , S_{c1} , S_{c2} , and S_{c3} are ON, and S_{2a} , S_{2b} , and S_{2c} are OFF, V_{in} is sampled at C_S . When clock ϕ_2 is high, S_{1a} , S_{c1} , S_{c2} , and S_{c3} are OFF, and one of the three switches, S_{2a} , S_{2b} , and S_{2c} , selected by the decoder is ON. Then, open-loop amplifier magnifies V_{in} to V_{out} .

Designing an open-loop amplifier in pipelined ADCs is deliberated on three aspects.

1) *Capacitive Attenuation*: The parasitic capacitance of the input node of the open-loop amplifier attenuates the input voltage due to charge sharing. Shown in Fig. 5(a), when V_i is sampled in C_S , and node X is reset to ground, the parasitic capacitance, C_P , has no effect on the sampling mode. However, in amplification mode [Fig. 5(b)], the charge in C_S is shared by C_P , and the voltage of node X can be derived as

$$V_X = - \left(\frac{C_S}{C_S + C_P} \right) \left(V_i - \frac{V_{REF}}{2} \times D_i \right). \quad (9)$$

Therefore, the open-loop amplifier must compensate the attenuation of $C_S/(C_S + C_P)$.

2) *Circuit Elaboration*: Fig. 6(a) shows a differential amplifier with source degeneration. The small-signal model in (10) can be approximated to the amplifier's behavior:

$$V_{out} = \frac{g_m R_D}{1 + g_m R_S} V_{in} \quad (10)$$

if the body effect is neglected. The source degeneration resistor R_S improves the linearity of the amplifier. Although the nominal gain of the open-loop amplifier is 2, the overall gain with capacitor networks is altered by the parasitic capacitive voltage division. To compensate the unknown gain reduction, the gain of the amplifier itself must be tunable. From (10), the voltage

only shift DC level of the amplifier but also provide buffering to extend the operating speed of the gain stage. Furthermore, the source follower shifts the output voltage down by $(V_{TH} + V_{OV})$, where V_{TH} is the threshold voltage and V_{OV} is the over-drive voltage. Then, the input common-mode voltage can be designed to yield the same output common-mode voltage.

3) *Linearity Effect*: The differential open-loop amplifier in the gain stage exhibits an “odd-symmetric” input/output charac-

Fig. 8. Open-loop amplifier. (a) Input-output transfer curves. (b) Corresponding gains.

Fig. 7. Simulated SNDR of ADC versus THD of open-loop amplifier.

teristic. The Taylor expansion of the characteristic in the range of interest can be expressed as

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) + \alpha_5 x^5(t) + \dots \quad (11)$$

Because the cubic term of (11) dominates the linearity of the ADC's performance, the higher order terms in the behavioral model are neglected for simplicity. Fig. 7 shows the signal-to-noise-plus-distortion ratio (SNDR) of the 6-bit ADC versus total harmonic distortion (THD) of the gain stage, where α_1 is equal to two, α_3 is varied from 0 to -33 , and the amplitude of input signal is 0.2 [10]. The simulation indicates that less than 2.1% THD is required in the open-loop amplifier for the proposed 6-bit ADC.

Fig. 8(a) and (b) shows HSpice simulation results of the open-loop amplifier input/output transfer curves and their corresponding gains for different V_{ctrl} . Parameters in this design are $R_D = 500 \Omega$, $g_m = 9 \text{ mA/V}$, and $R_S = 11 \sim 150 \Omega$. By performing curve fitting for V_{out} between -0.2 V and 0.2 V , their parameters are shown in Table I, where G_{att} represents

TABLE I
CURVE-FITTING PARAMETERS AND SIMULATION RESULTS

V_{ctrl}	α_1	α_3	G_{att}	$\alpha_3 G_{att}^3$	SNDR	THD
0.75 V	2.39	-5.83	0.85	-3.60	37.26 dB	0.43 %
0.80 V	2.89	-8.26	0.70	-2.86	37.35 dB	0.42 %
0.90 V	3.43	-11.42	0.59	-2.34	37.40 dB	0.39 %
1.80 V	3.99	-16.07	0.51	-2.08	37.44 dB	0.37 %

the attenuation factor, V_{in} is the input voltage before capacitive attenuation, and V_{out} is the amplifier output. From (11), the output of the amplifier is expressed as

$$\begin{aligned} V_{out} &= \alpha_1 \cdot G_{att} V_{in} + \alpha_3 \cdot (G_{att} V_{in})^3 \\ &= \alpha_1 G_{att} \cdot V_{in} + \alpha_3 G_{att}^3 \cdot V_{in}^3. \end{aligned} \quad (12)$$

Table I indicates that higher V_{ctrl} results in larger α_3 . However, the overall coefficient of cubic term is attenuated by G_{att}^3 such that the output swing is constant. If the gain of the open-loop amplifier needs to be high, it means the effective input swing is small. Therefore, the nonlinearity is softened by the attenuation. Behavioral simulation results of the proposed ADC in Table I show that the performance is quite constant for the tunable control voltage range.

C. Comparator

To reduce static power consumption, this ADC applies dynamic comparators in the pipelined stage. Shown in Fig. 9, the comparator consists of an input differential pair M_1 – M_2 and a back-to-back inverter latch M_3 – M_6 . Input parasitic capacitances of the differential pair will result in the memory effect of previous input value, thereby affecting the detection of the comparison. To eliminate this effect, switches reset these nodes when comparators are in sampling mode. The outputs of the dynamic comparator pass through a static latch to eliminate glitch and reduce sensitivity to meta-stability. Accordingly, the compared results are decoded into the digital code and control signals of switches in pipelined stages.

Fig. 9. Comparator.

(a)

(b)

Fig. 10. (a) Gain-control servo loop. (b) Error amplifier.

D. Global Gain Control

Because the parasitic capacitance cannot be modeled precisely, a servo loop, shown in Fig. 10(a), is required to com-

Fig. 11. Behavioral simulation of SNDR versus stage gain.

pensate the gain error. The duplicated residue amplifier serves as a replica circuit for the pipelined stages in this ADC. Since the layout of the residue amplifier circuit is identical to those in pipelined stages, these parasitic capacitances are approximately the same. The operation of the servo loop is as follows. The amplifier samples $V_{REF}/2$ at clock ϕ_1 . Then, the open-loop amplifier magnifies the sampled signal to obtain the output for comparison at clock ϕ_2 . Switches at the output of the open-loop amplifier are *ON* during ϕ_2 and are *OFF* during ϕ_1 . Thus, these switches perform peak detection to sample the magnitude of the amplified value. Then, the sampled value is compared with V_{REF} by an error amplifier to obtain the amplified voltage error. With an external RC low-pass loop filter, the control voltage (V_{ctrl}) is fed back to the gate of M_R in Fig. 6(b) for global gain control. Fig. 10(b) shows the schematic of the error amplifier. Since the external RC low-pass filter (LPF) dominates the loop bandwidth, the error amplifier only acts as a gain stage to amplify the error signal. Thus, the settling time and phase margin of the error amplifier are not as stringent as in a normal operational amplifier. Consequently, the global gain control circuit only needs to operate in low frequency while open-loop amplifiers can operate at high-frequency conversion. Shown in Fig. 11, the behavioral simulation shows the gain error must be kept within 5% to ensure 6-bit accuracy. The DC gain of the error amplifier is conservatively designed to about 46 dB. An off-chip LPF with resistor ($R_G = 30 \text{ k}\Omega$) and capacitor ($C_G = 20 \text{ pF}$) suppresses the high-frequency components of the error amplifier output and presents the control signal to open-loop amplifiers. In HSpice simulation, the control signal settles within 380 ns.

E. Digital Error Correction and Decimation

To provide a reliable digital output interface, the digital output is decimated to enable reliable acquisition by a logic analyzer. Since the pipelined ADC converts data at two interleaved banks, the decimation number must be odd to avoid sampling from the same bank. Based on these considerations, the decimation number is chosen as 21. For example, if the original output sequence of *Bankx* and *Banky* is interleaved as 1, 2, 3,...

Fig. 12. (a) Decimation timing. (b) Decimation output block.

Fig. 13. Output SNDR for (a) offset mismatch, (b) gain mismatch, and (c) phase mismatch at 800 Msample/s.

in Fig. 12(a), the decimated sequence is 4, 25, 46, 67, ... In order for the decimated output to keep the interleaved relationship, two signals, x_{sel} and y_{sel} , select the output of original sequence as $x/21$ and $y/21$ in Fig. 12(a). Finally, a control signal, $muxsel$, selects the inputs of the multiplexer

to derive the output data, DO . The decimated clock, CKO , provides added convenience for data acquisition. Fig. 12(b) shows block diagram of corresponding output. All digital circuits are synchronous to avoid the need for accounting latency differences.

Fig. 14. (a) Layout between PADS and THAs. (b) Interleaved layout.

Fig. 15. ADC microphotograph.

IV. DESIGN CONSIDERATIONS

The time-interleaved ADC is sensitive to mismatches in offset, gain, and phase [11]–[14]. In a 6-bit 800 Msamples/s pipelined ADC's behavioral simulation, the effects of mismatch in offset, gain, and phase are shown in Fig. 13. To achieve better than 5-bit performance, the offset, gain, and phase mismatch must be less than 3.8% of the full-scale input, 4.5%, and 18 ps, respectively.

In physical layout, the phase mismatch arises from different propagation delay between pads and input of two interleaved sampling capacitors. Shown in Fig. 14(a), the 100- Ω resistor matches the output impedance of signal source to avoid the reflection. The routing between pads and the inputs of the two THAs is as short and symmetric as possible. Therefore, input

Fig. 16. Measured INL and DNL.

resistance including switches is approximately 100 Ω . With 300-fF input capacitance, the time constant is about 30 ps and the mismatch can be easily kept within 18 ps corresponding to the requirement in Fig. 13(c). In addition to input delay mismatch, the mismatch of two nonoverlapped clocks induces phase mismatches. Since the even duty cycle is important for interleaving, the input clock is divided by two to obtain the 50% duty cycle clock. In the layout, loading of two paths are balanced to meet the requirement. To alleviate the gain mismatch and offset mismatch, the two banks of pipelined stages interlace each other as shown in Fig. 14(b). The capacitors and guard rings isolate the analog part from noisy switching in this topology.

Fig. 17. (a) FFT of 100 MHz at 800 Msample/s. (b) FFT of 399.9 MHz at 800 Msample/s.

Fig. 18. (a) SNDR and SFDR versus conversion rate with 100 MHz input. (b) SNDR and SFDR versus input frequency at 800 MS/s.

IR drops of power lines in the layout affect gain accuracy of open-loop amplifiers. However, one advantage of pipelined ADCs is that gain-accuracy requirements in rear stages are lower than front stages. Thus, the replica circuit in the servo loop is placed near the first stage to lower the sensitivity of gain variation. The power lines are composed of metal 4 and metal 6 with the width of 20 μm in parallel, and the power pads are near the first stage. Because metal 6 is a thick layer, power-line resistance across the pipelined ADC is within 0.3 Ω . In addition, current routing of local bias reduces the problems with mismatch and power-line resistance by reducing the distance in the current mirror [15].

V. EXPERIMENTAL RESULTS

Fig. 15 shows the microphotograph of the ADC chip. This chip occupies $1 \times 1.2 \text{ mm}^2$ and the active area is 0.5 mm^2 . It has been fabricated in a 0.18- μm CMOS technology. Power lines of analog, digital, clock, and output blocks are separated and connected to on-chip decoupling capacitors to avoid the wire bouncing and noise coupling. Only one 1.8-V power supply is required for this chip.

In high sample-rate systems a clean, low-jitter clock source must be employed. The input signal amplitude is 400 mVpp, input common-mode voltage is 1.3 V, and the decimated output is *DO*, as depicted in Fig. 12(a).

Integral nonlinearity (INL) and differential nonlinearity (DNL) are calculated based on code-density measurement on the combined signal from both channels in Fig. 16. With a 100-MHz sinusoidal signal at 800-Msample/s conversion rate, peak INL is 0.36 LSB, and peak DNL is 0.41 LSB. Fig. 17 shows the output spectrum of the converted data at 800 Msample/s. The spectrum of the sampled signal is folded between 0 to 19 MHz because of decimation by 21. With a 100-MHz input, SNDR and spurious-free dynamic range (SFDR) of the ADC are 33.7 dB and 47.5 dB, respectively. Near Nyquist sampling, SNDR and SFDR of the ADC still maintain above 31.5 dB and 37.5 dB, respectively.

The ADC's dynamic performance is measured by varying the sampling rate from 200 Msample/s to 1 Gsample/s. Shown in Fig. 18(a), with the input signal frequency of 100 MHz, the effective number of bits (ENOB) is better than 5.3 up to 800 Msample/s. In higher conversion rate, the output voltage of the open-loop amplifier cannot settle within the desired level.

TABLE II
6-bit ADC FOM COMPARASION

Author/year	Architecture	Technology (μm)	Fs (MHz)	ENOB (bit)	ERBW (MHz)	Power (mW)	FOM (pJ/step)
Sander'05 [17]	Flash	0.13	1200	5.7	700	160	2.2
Jiang'05 [3]	Interleaved Flash	0.18	2000	5.55	941	310	3.5
Draxelmayr'04 [7]	Interleaved SAR	0.09	600	5.35	300	10	0.4
Uyttenhove'03 [18]	Flash	0.25	1300	5.35	550	600	13.4
Scholtens'02 [19]	Flash	0.18	1600	5.7	610	328	5.17
Geelen'01 [16]	Flash	0.35	900	5.65	450	200	4.4
Choi'01 [2]	Flash	0.35	1000	5.7	650	500	7.4
This work	Interleaved Pipelined	0.18	800	5.35	460	105	2.8

TABLE III
PERFORMANCE SUMMARY

Technology	TSMC 0.18 μm CMOS
Chip Area / Active Area	1.2 mm ² / 0.5 mm ²
Resolution	6 bits
Conversion Rate	800 MS/s
INL / DNL	0.36 LSB / 0.41 LSB
Input Range	400 mV _{p-p} differential
SFDR @ fin=100 MHz	47.5 dB
SNDR @ fin=100 MHz @ fin=400 MHz	33.7 dB 31.5 dB
Power Dissipation	analog : 75 mW digital : 30 mW
Supply Voltage	1.8 V

Therefore, the global gain control mechanism must increase the voltage gain of the amplifier. When the required gain is beyond the control range of servo loop, the performance degrades. Accordingly, the SNDR of the ADC descends at the sampling frequency over 800 Msample/s. When the sampling rate is fixed at 800 Msample/s, SNDR and SFDR with various input frequencies are plotted in Fig. 18(b). Since SNDR and SFDR drop slightly above Nyquist frequency, the performance is quite constant for the input signals with wide frequency range. Excluding output buffers, this ADC consumes 75 mW for analog circuits and 30 mW for the rest of digital circuits at 800 Msample/s. The figure of merit (FOM) calculated by the definition of (13) [16] is 2.8 pJ.

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot 2 \cdot \text{ERBW}} \quad (13)$$

where ERBW is effective resolution bandwidth. Table II shows the FOM comparison of 6-bit ADCs. The measured performance summary is shown in Table III.

VI. CONCLUSION

The combination of voltage-mode open-loop amplifiers and two-bank interleaving in pipelined architecture realizes a 6-bit pipelined ADC achieving 800 Msample/s without the need of digital calibration. The servo loop of global gain control compensates the gain attenuation by parasitic capacitances. Applying global gain control relaxes the stringent requirement of high-gain amplifier design and allows the pipelined ADC with open-loop amplifiers to operate at high-conversion rate. This approach extends the conversion speed of designing a pipelined ADC in low-voltage and low-power applications for nano-meter technologies.

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