The Design and Analysis of a DLL-Based Frequency Synthesizer for UWB Application

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Abstract—A delay-locked loop (DLL)-based frequency synthesizer is designed for the ultrawideband (UWB) Mode-1 system. This frequency synthesizer with 528-MHz input reference frequency achieves less than 9.5-ns settling time by utilizing wide loop bandwidth and fast-settling architecture. Additionally, a discrete-time model of the DLL and an analytical model of phase noise of the delay line are proposed in this work. Experimental results show great consistency with predicted settling time and phase noise. The circuit has been fabricated in a 0.18- μm CMOS technology and consumes only 54 mW from a 1.8-V supply. It exhibits a sideband magnitude of -35.4 dBc and -120 -dBc/Hz phase noise at the frequency offset of 1 MHz.

Index Terms—Delay-locked loops, frequency multiplier, phase noise.

I. INTRODUCTION

THE UWB system utilizes the unlicensed 3.5–10 GHz band with a strict regulation in emission power less than -41 dBm by the Federal Communications Commission (FCC). The Multi-Band OFDM Alliance (MBOA) proposed a frequency-hopping spread-spectrum (FHSS) communication system, and the frequency plan is shown in Fig. 1. Frequency bands belonging to group 1 are for the earlier Mode-1 operation [1].

The difficulty of generating the desired frequency arises from the stringent specification of 9.5-ns band-hopping time. For the conventional phase-locked loop (PLL)-based frequency synthesizer, it takes hundreds of reference cycles to settle down. In order to settle the loop within 9.5 ns, the reference frequency must be in the order of tens of GHz, thereby obviating this approach.

Most of the reported approaches [1]–[3] generate three carrier frequencies for MBOA-UWB system by single-sideband (SSB) mixers. However, the SSB mixers have many inherent drawbacks such as high power and spurious tones. The local oscillator (LO) leakage and the unwanted sideband translate adjacent interferences to the baseband and corrupt the signal at the desired channel. All foregoing nonideal effects degrade the performance of the UWB transceiver severely.

In Section II, a delay-locked loop (DLL)-based frequency multiplier [4] is proposed to generate the three carrier frequencies. Then, Section III describes the design considerations analytically, including settling time, spurs, and phase noise. Sec-

Fig. 1. Frequency plan of MBOA-UWB system.

tion IV illustrates the major building blocks of this architecture and Section V shows experimental results and summarizes with a conclusion.

II. ARCHITECTURE OF THE DLL-BASED FREQUENCY MULTIPLIER

The frequency multiplication factor of a conventional DLL-based frequency multiplier is the number of delay cells [5]. To synthesize different carrier frequencies, the voltage-controlled delay line (VCDL) must exhibit the characteristics of variable delay. Shown in Fig. 2(a), the equivalent delay can be changed by switching the feedback clock from one delay cell to another. Therefore, the output frequency will be changed to a different band consequently because the multiplication factor equals to the number of delay cells.

The DLL is a first-order system in nature and its loop bandwidth can be relatively wide without stability problems. If the loop bandwidth can be wide enough, it can settle down within 9.5 ns.

However, direct switching between different delayed reference clocks causes the undesired glitch shown in Fig. 2(b). If the frequency multiplier switches from ϕ_{13} , the output clock of the 13th delay cell, to ϕ_{15} , the output clock of the 15th delay cell, an undesired glitch may appear. The appearance of the undesired glitch confuses the phase detector (PD) because it produces an extra UP/DN pulse and changes the delay of the feedback clock significantly. The possible incorrect detection of the PD increases settling time and the frequency multiplier needs an extraneous long time to return to the normal state. To resolve the long-settling problem, multiple PDs and charge pumps are utilized and the circuit chooses the corresponding PD/charge pump for each band accordingly.

Fig. 3 shows the architecture of the proposed DLL-based frequency multiplier where the blocks inside the dash box are not implemented in this work. A 528-MHz reference frequency can be generated by a conventional PLL-based integer-N frequency synthesizer. The bandwidth of the nonswitching PLL-based synthesizer can be optimized for the phase noise.

To determine the number of delay cells for the DLL-based frequency multiplier, the carrier frequencies are decomposed and listed in Table I. Three different frequencies have a maximum

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Fig. 2. (a) Conventional DLL-based frequency multiplier. (b) Switching glitch.

Fig. 3. Proposed synthesizer architecture.

common factor, 264 MHz, and the number of delay cells is 13, 15, and 17, respectively. However, the loop bandwidth of the DLL is directly constrained by the frequency of the reference clock. Because a reference clock of 264 MHz cannot guarantee sufficient loop bandwidth, 528 MHz, two times of 264 MHz, is chosen as the reference clock, and consequently the output of the edge combiner must be divided by 2 to obtain desired output frequencies. Another advantage of this frequency multiplier is that it produces quadrature clocks to provide local oscillators for a direct-conversion transceiver, a most likely architecture for low-cost UWB applications.

The 2-bit select signal in Fig. 3 selects the feedback clock, switches the charge pump and tunes the edge combiner to the corresponding frequency for the DLL to synthesize different frequencies. The open-loop gain must be chosen properly such that the frequency multiplier can achieve a settling time less than

TABLE I
DECOMPOSITION OF FREQUENCIES

Carrier Frequency	Decomposition
3432 MHz	264 X 13 MHz
3960 MHz	264 X 15 MHz
4488 MHz	264 X 17 MHz

Fig. 4. DLL discrete-time model.

9.5 ns. The matching between different delay cells in the VCDL is critical here and can be done with careful layout.

III. DESIGN CONSIDERATION

A. Settling Time Analysis

DLLs can be modeled in the s domain if its loop bandwidth is much narrower than the input reference frequency. However, the loop bandwidth of the proposed DLL must be wide enough for fast settling. Therefore, a more accurate model must be used to analyze time-domain response.

DLL operates in a discrete-time domain inherently. Shown in Fig. 4, t_{err} represents the instantaneous time error at the instant when the feedback signal is switched from one delayed reference clock to another. At the same time, the reference clock remains unchanged, and, hence, no input phase error appears. The input time error, t_{out} , will eventually appear at the output of the VCDL. The combination of the charge pump and the loop filter is modeled as $K_{CHP}/(1-z^{-1})$ in a discrete-time system, where the constant gain block K_{CHP} is equal to the charge-pump current I_C . The current signal is then converted to the voltage signal by the loop filter and controls the VCDL whose gain is equal to K_{VCDL} . When the DLL is approaching lock, the time delay from the input of the VCDL to the output of the VCDL equals to the period of the reference clock T_p .

The open-loop gain K can be expressed as

$$K = \frac{K_{CHP} \cdot K_{VCDL}}{C_p}. \quad (1)$$

The transfer function can be written as

$$\frac{t_{out}(z)}{t_{err}(z)} = \frac{-K}{1 - (1 - K) \cdot z^{-1}} \quad (2)$$

which is a first-order system. The switching in the feedback signal can be viewed as a phase step input which appears at the feedback path. This phase step input can be expressed as

$$t_{err}(n) = \theta_o \cdot u(n). \quad (3)$$

The z -transform of (3) is

$$t_{\text{err}}(z) = \frac{\theta_o}{1 - z^{-1}}. \quad (4)$$

The output time error is described as

$$t_{\text{out}}(n) = -\theta_o \cdot (1 - (1 - K)^{n+1}) \cdot u(n). \quad (5)$$

The open-loop gain K must be larger than 0 and smaller than 2 for the consideration of the system stability.

If the output phase error must settle to within 99% of input phase error, the loop gain for the required settling time can be calculated as follows. The output phase error is

$$t_{\text{out}}(n_o) = 0.99 \cdot \theta_o. \quad (6)$$

Equation (5) can be rewritten as

$$K = 1 - \exp\left(\frac{1}{1+n} \ln(0.01)\right). \quad (7)$$

The reference frequency corresponds to 1.9 ns, thus allowing five reference cycles for settling. To settle the DLL within five reference cycles, the loop gain K needs to meet the constraint

$$K \geq 0.54. \quad (8)$$

According to the foregoing analysis, the settling time of a wide loop bandwidth DLL can be accurately predicted, and the stability criterion is also obtained. The open-loop gain is set to 0.6 in this work for the consideration of settling time.

B. Spur Analysis

When the DLL is locked, each delay cell shifts the phase of the reference clock by $2\pi/N$ (rads). Fig. 5(a) shows that each output signal coming from a delay cell is represented by a vector for $N = 5$. Each signal from the delay cell is evenly phase-spaced and all higher order harmonic tones can be suppressed except the N -th harmonic tone. The frequency of the output signal is therefore multiplied by N . Nevertheless, random mismatches of N delay cells drive the actual phase of the delayed clock to deviate from the ideal phase. The phase error between the actual and the ideal phase can be approximated as in Fig. 5(b) for small time error. The amplitude of the erroneous phase can be expressed as

$$A_k = A_{\text{ref}}/k \quad (9)$$

$$A_{\text{err}} = k \cdot A_k \cdot \theta_{\text{err}}. \quad (10)$$

In (9), A_k is the amplitude of the k th harmonic, and A_{ref} represents the amplitude of the reference clock. Equation (10) indicates that the erroneous amplitude A_{err} for the k th harmonic due to phase error θ_{err} is equal to k times $A_k \cdot \theta_{\text{err}}$. Therefore, for a fixed θ_{err} , the signal-to-distortion ratio of the output of the edge combiner is independent of the multiplication factor N . Additionally, because the ideal phase and erroneous phase in Fig. 5(b) are orthogonal to each other, the erroneous phases are equally phase-spaced. Therefore, they will be partially cancelled out, reducing the magnitude of the spurs.

Fig. 5. (a) Vector diagram for N equal phase-spaced signals. (b) Approximation of phase error.

Fig. 6. Distribution of spur level.

In Fig. 6, for 1% phase-error variance in delay cells, Monte Carlo simulations in MATLAB show that the proposed frequency synthesizer can yield a lower spur level than conventional SSB mixers. Furthermore, the error in the 13-stage delay cells tends to “average” the mismatch effect. Therefore, the proposed frequency synthesizer can yield better spur distribution. Note that the spur level is highly reliant on the layout technique, and can be improved by careful layout.

C. Phase Noise Analysis

The phase noise of a DLL-based frequency multiplier is inherently better than its counterpart, the PLL-based frequency synthesizer. The impulse sensitivity function (ISF) in [6] is used to analyze the phase noise of the delay cell. Fig. 7 shows the waveform and the corresponding ISF of a typical ring oscillator and a delay cell. Similar to the operation of an oscillator, the noise impulse disturbs the phase of the delay cell only during its transition. Fig. 8 shows the most significant difference between a voltage-controlled oscillator (VCO) and a delay cell.

Fig. 7. Waveform and ISF of (a) a typical ring oscillator and (b) a delay cell.

Fig. 8. Phase disturbance present in (a) a typical ring oscillator and (b) a delay cell.

The delay cell in a three-stage ring oscillator is triggered by its preceding delay stage. The waveform of the output signal is shown in Fig. 8(a). A phase disturbance in the preceding edge passes to the following delay stage. The process persists and the phase disturbance disrupts the oscillation waveform permanently. As shown in Fig. 8(b), a delay cell is triggered by a clean reference signal and the phase disturbance in a transition edge is reset to zero when the next edge comes.

If the transition edge of the delay cell is contaminated by a random noise as shown in Fig. 9(a), the relationship between a random timing error Δt and a noise voltage ΔV is given by

$$\frac{\Delta t}{\Delta V} = \frac{1}{\text{SR}} \quad (11)$$

where SR is the slew rate of the output voltage from the delay cell.

The ISF of the delay cell is like a delta function. The amplitude depends on the time τ when the noisy current impulse is injected. Unlike the ISF of a VCO, the ISF of a delay cell is not periodic because of the resetting operation carried out by the reference signal. Therefore, the impulse response for excess phase of the delay cell can be expressed as

$$h_\phi(t, \tau) = \Gamma(\tau) \cdot [u(t - \tau) - u(t - \tau')] \quad (12)$$

where τ' is the zero crossing time and $\Gamma(\tau)$ is the ISF of the delay cell. For a constant slew rate, the integrating period can be approximated to be the rising or falling time of the delayed reference clock as shown in Fig. 9(b). Therefore, (12) can be approximated as

$$h_\phi(t) = \frac{i_n \cdot T_s}{C_L \cdot \text{SR}} \quad (13)$$

Fig. 9. (a) Relation between noise voltage and timing error. (b) Noise impulse at the transition.

where i_n is the noise current of the device, T_s is the rising or falling time of the delayed reference clocks, and C_L is the output capacitance.

Given the phase uncertainty as shown in (13), the output waveform can be expressed as

$$V_{\text{out}} = A \cdot \cos(\omega(t + h_\phi(t))) \quad (14)$$

where A is the amplitude of the output signal. Equation (14) can be further simplified to

$$V_{\text{out}} \cong A \cdot \left[\cos(\omega t) - \frac{i_n(t) \cdot T_s \cdot 2\pi}{C_L \cdot \text{SR} \cdot T_{\text{ref}}} \cdot \sin(\omega t) \right] \quad (15)$$

Suppose that a noise current $i_n(t)$ is injected into the output node at a frequency of $\Delta\omega$ less than ω_0 .

$$i_n(t) = I_o \cos(\Delta\omega t) \quad (16)$$

where I_o is the amplitude of $i_n(t)$. The phase disturbance is transformed to the voltage disturbance, which can be expressed as

$$V_{\text{SBC}} = A \cdot \left[\frac{I_o \cdot \cos(\Delta\omega t) \cdot T_s \cdot 2\pi}{C_L \cdot \text{SR} \cdot T_{\text{ref}}} \cdot \sin(\omega t) \right] \quad (17)$$

$$= A \cdot \left[\frac{1}{2} \cdot \frac{I_o \cdot T_s \cdot 2\pi}{C_L \cdot \text{SR} \cdot T_{\text{ref}}} \cdot \sin((\omega \pm \Delta\omega) \cdot t) \right] \quad (18)$$

Therefore, a pair of equal sideband spurs at $\omega \pm \Delta\omega$ produced by a single-tone noise is equal to

$$P_{\text{SBC}}(\Delta\omega) = 10 \cdot \log \left(\frac{I_o \cdot T_s \cdot \pi}{C_L \cdot \text{SR} \cdot T_{\text{ref}}} \right)^2 \quad (19)$$

The power of the phase noise in a delay cell is constant with respect to the offset frequency, $\Delta\omega$. However, the power of phase noise in a VCO is given by

$$P_{\text{SBC}}(\Delta\omega) = 10 \cdot \log \left(\frac{I_o \cdot c_n}{4 \cdot q_{\text{max}} \cdot \Delta\omega} \right)^2 \quad (20)$$

which is proportional to $1/\Delta\omega^2$. Such difference resulted from the fact that the VCO preserves previous phase disturbances and the integrating period spans from the beginning of the oscillation to the present instance.

Equation (19) predicts that only two regions, $1/f^1$ and $1/f^0$ slope regions, exist in the phase noise spectrum of a delay cell. The $1/f^1$ region is the “flicker noise” region, because the timing uncertainty is caused by the device flicker noise. The spectrum

Fig. 10. (a) Sideband power with different slew rate. (b) Sideband power with different reference period.

falls just as the flicker noise in $1/f^1$ slope. The $1/f^0$ region is the “thermal noise” region, since the phase disturbance is originated from the device thermal noise. The spectrum is as flat as the white thermal noise.

The theoretical prediction is verified by simulation results. A sinusoidal current of $50 \mu\text{A}$ is injected into the output node of the delay cell to emulate the interaction between the noise current and the delayed reference signal. Fig. 10(a) shows the comparison between the prediction and the simulation result. The dash line represents the predicted value and the solid line stands for the simulation results. The simulation is performed in HSPICE by altering the slew rate of the delayed reference signal. Equation (19) predicts that the sideband power drops in 40 dB per decade slope, since the transition time, T_s , doubles as the slew rate is reduced to half. Fig. 10(b) illustrates that the sideband power drops in 20 dB per decade slope as the reference period increases, in good agreement with the simulation.

The phase noise of the input clock needs to be considered for more accurate prediction of the overall noise. Because the input phase noise is directly added to the overall phase noise of the delay line, it is chosen about the same phase noise level of each delay cell, such that it contributes negligible effects on the synthesized clock output.

IV. CIRCUITS

A. Delay Cell

Shown in Fig. 11, the delay cell is a single-ended inverter, consisting of M_2 and M_3 in series with M_1 and M_4 operating in the triode region [7]. The delay of the circuit is determined by the equivalent resistance of M_1 and M_4 , controlled by V_c . An additional inverter comprising M_5 and M_6 serves as an output buffer for higher frequency operation. The circuit performs a rail-to-rail operation, so it consumes no static power.

Nevertheless, differential signals are preferable for the common-mode rejection. Cross-coupled inverters are utilized

Fig. 11. (a) Current-starved delay cell. (b) Pseudo-differential delay cell.

to regulate differential outputs to perform the pseudo-differential operation [8]. Besides, because a clock with 50% duty cycle is critical for the spur level of the synthesized output, proper choice of the size of cross-coupled inverters can perform duty cycle correction. In this work, the size of the cross-coupled inverter is chosen about one-third of that of the inverter in the delay cell to yield the best performance.

B. Edge Combiner

The edge combiner synthesizes desired output frequencies based on the multiple-phase outputs of the DLL [5]. Shown in Fig. 12, the differential pairs convert voltage signals to current signals and sum up at the output node. The output load comprises a variable LC-tank to tune the center frequency of the tank by the switched-capacitor array. Due to 1.5-GHz wideband operation, variable tank frequency is required to maintain output signal power for all three bands. The quality factor of the tank is less important in this edge combiner, because the phase noise is dominated by the noise of the input reference clock and delay cells rather than by the quality factor Q of the inductor. The quality factor of the inductor is chosen to be 10 here to achieve adequate output swing with a small current consumption.

C. PD and CHP

To enhance common-mode rejection, a pseudo-differential dynamic phase detector (PD) compares the phase of the reference clock with the feedback clock. The pseudo-differential PD consists of a positive-edge triggered PD and a negative-edge triggered PD as shown in Fig. 13. Two complementary PDs with equal input to output time delay produce differential UP/DOWN control signals. This architecture has a benefit of high speed over static PD. Shown in Fig. 14, a differential charge pump with a unity-gain feedback amplifier, in which the differential-to-single operational amplifier determines the output

Fig. 12. Edge combiner with a tunable load.

Fig. 13. Pseudo-differential PD.

Fig. 14. Differential charge pump circuits.

common-mode level by itself, is realized for high-speed operation. The effect of charge sharing can be alleviated by the differential operation, and the static phase error is reduced consequently.

D. Frequency Divider

A divide-by-2 divider takes the output from the edge combiner and generates quadrature outputs. A static divided-by-2 divider, shown in Fig. 15, is used in this work to generate all

Fig. 15. Divide-by-2 frequency divider.

Fig. 16. Die photo.

three frequencies. Operating at the frequency up to 9 GHz, current-mode logic (CML) is used in this divider.

V. EXPERIMENTAL RESULTS

The DLL-based UWB clock generator has been fabricated in a 0.18- μm CMOS technology. Fig. 16 is a photograph of the die, whose area is 0.98 mm by 0.8 mm. The circuit has been tested by a chip-on-board assembly while running at the input frequency of 528 MHz from a 1.8-V power supply. Fig. 17 shows the output spectrum of the clock generator for the carrier frequency at 3432 MHz. The adjacent channel spur suppression is about -35.4 dB.

The switching time of this clock generator is measured at the sampling scope. The channel control signal is toggled by a 6-MHz pulse. Fig. 18 shows that the clock generator can switch between two adjacent channels within 8 ns.

The overall flicker noise of 13-stage delay cells is equal to 13 times the predicted noise in (20). The 528-MHz input reference clock, the synthesized frequency of 3432 MHz and the predicted phase noise are shown in Fig. 19. The phase noise of the synthesized clock is measured at -120 dBc/Hz at 1-MHz frequency offset, consistent with the predicted phase noise. The measured performance of the proposed synthesizer is also summarized in Table II together with that of the most recent works on UWB clock generators.

Fig. 17. Output spectrum at 3432 MHz.

TABLE II
PERFORMANCE SUMMARY

	[9]	[10]	This Work
Process	0.25- μ m SiGe	0.13- μ m CMOS	0.18- μ m CMOS
Power	73.4 mW / 2.7 V	30 mW / 1.3 V	54 mW / 1.8 V
Sideband Spur	-35 dBc	-27 dBc	-35 dBc
Phase Noise @ 1 MHz (dBc/Hz)	-100	-104	-120
Die Size (Core Area)	1 mm ²	N.A	0.3 mm ²

VI. CONCLUSION

This paper has presented a DLL-based frequency multiplier for UWB application with thorough analysis. The frequency synthesizer can generate three carrier frequencies for the MBOA-UWB system and is able to switch between different channels within 9.5 ns. The system requires only two inductors and the compact structure is suitable for low-cost UWB applications.

The phase noise model for the DLL-based frequency multiplier is developed and experimental results show the consistency between the theory and the experiment. The system achieves a low phase noise of -120 dBc/Hz at 1-MHz offset frequency while dissipating only 54 mW from a single 1.8-V power supply.

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Fig. 18. Settling behavior for channel switching.

Fig. 19. Measured and predicted phase noise.

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