A Broadband Balanced Distributed Frequency Doubler With a Sharing Collector Line

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Abstract—A broadband balanced distributed frequency doubler fabricated by 0.35 μm SiGe BiCMOS technology is developed to operate from 4 to 18 GHz output frequency. This balanced doubler consists of an active balun and a distributed doubler. A sharing collector line is used in the balanced distributed doubler to reduce the chip size. This circuit exhibits a measured conversion loss of less than 8 dB and a fundamental rejection of better than 23 dB for the output frequency between 4 and 18 GHz. The chip size is 1.1 × 0.7 mm².

Index Terms—Balanced doubler, distributed doubler, SiGe BiCMOS.

I. INTRODUCTION

RECENTLY, the strong demand for high-speed wireless communication systems requires broadband and high-quality frequency sources. An oscillator cascaded with a frequency multiplier can relax the requirements of the local oscillation (LO) source. Therefore, broadband frequency multipliers are the important components in high-speed wireless communication systems.

Broadband frequency doublers can be implemented by distributed topology [1]–[3]. In order to achieve a good fundamental rejection, distributed doublers with a high-pass drain line were proposed, however, the operation bandwidth is limited due to the output high-pass filter [1], [2]. The balanced structure can also be applied to design a broadband frequency doubler with a good fundamental rejection. A GaAs HEMT balanced distributed doubler that consists of a reduced size rat-race coupler and two identical distributed doublers demonstrated a conversion gain between −3 and −6 dB from 30 to 50 GHz output frequency, but it requires a 10 dBm input power and 132 mW dc power [3]. An InGaP heterojunction bipolar transistor (HBT) balanced doubler with active balun has a 10 dB average conversion gain between 14 to 24 GHz output frequency and consumes 200 mW dc power [4]. The Gilbert-cell topology is also suitable for the balanced doublers [5], [6]. A dc to 86 GHz InP DHBT doubler presents a conversion gain between −3 and −6 dB and consumes 730 mW dc power [6]. Most of the previously reported broadband balanced frequency doublers require high power consumption.

In this letter, a broadband balanced distributed doubler with active balun is developed by using TSMC 0.35 μm SiGe BiCMOS technology. The distributed doubler with two identical base lines and a sharing collector line is proposed to reduce the chip size. This doubler has a conversion gain better than −8 dB and the fundamental rejection is better than 23 dB from 4 to 18 GHz. The dc power consumption is 54 mW, and the chip size is 1.1 × 0.7 mm². This doubler demonstrates broadband characteristic and good fundamental rejection under a lower dc power consumption compared with other balanced frequency doublers.

II. CIRCUIT DESIGN

This circuit is fabricated by 0.35 μm SiGe BiCMOS process. This process provides three poly layers for the emitter and base of the SiGe HBTs and the gate of the CMOS transistors and three metal layers for interconnections. The HBT in this process has a $f_T$ of 70 GHz and a $f_{max}$ of 57 GHz. The MIM capacitor of 1 fF/μm² capacitance is also available in this technology.

The balanced distributed doubler is composed of an active balun and a distributed doubler. Fig. 1 shows the schematic of the active balun. The single-ended input signal is divided into two signals with equal magnitude and 180° phase difference by the active balun, and these two signals are fed to the transistors of the distributed doubler to generate the harmonic signals. The fundamental signals are cancelled and the second harmonic signals are in-phase combined at the output of the doubler.

Fig. 1. Schematic of the active balun.
The active balun consists of a differential pair, \( M_1 \) and \( M_2 \), for amplification, and the base of \( M_2 \) is connected to a bypass capacitor which provides a short circuit. The current source \( M_3 \) provides high impedance at \( S_1 \) to increase the common-mode rejection ratio (CMRR). The wideband input matching of the active balun is achieved by using a distributed topology that consists of two series inductors, the input equivalent capacitor of \( M_1 \) and a termination resistor. The inductive peaking is used at the output of the active balun to extend the operating frequency [7], [8].

To compensate the gain and the phase imbalances of the active balun, the \( L_3 \) and \( L_4 \) are selected to be 0.65 and 0.75 nH, respectively. Fig. 2 shows the simulated magnitude and phase imbalances of the active balun. Between 2 and 10 GHz, the magnitude difference is smaller than 1 dB and phase difference is between 175° and 180°. This active balun can provide a good single-to-differential function for the balanced doubler.

The balanced distributed doubler consists of a reduced size rat-race coupler and two identical distributed doublers was proposed in a chip size of 1.5 mm [3]. In order to reduce the chip size of the doubler, the balanced distributed doubler which is composed with two base lines and a sharing collector line is proposed, as shown in Fig. 3. Two transistor pairs are selected for this doubler, and each transistor pair has differential input at base terminals and the collectors of are connected together. The base line is designed with 50 Ω characteristic impedance for impedance matching. In addition to the impedance matching, a higher cut-off frequency of the collector line is required.

Smaller inductors of the collector line result in lower characteristic impedance and higher cut-off frequency. The 35 Ω collector line is selected in this design for compromising the impedance matching and operation bandwidth. The differential outputs of the active balun are connected to the two base lines of the distributed doubler to form the complete balanced distributed doubler. Fig. 4 shows the chip photo of the doubler, and the chip size of 1.1 mm × 0.7 mm.

### III. Measurements

The chip was measured using on-wafer probing. The transistors of the distributed doubler are biased near the pinch-off region. Fig. 5 shows the measured result of the conversion gain versus input power at input frequency of 4.5 GHz. It has maximum conversion gain of –3 dB at –7 dBm input power. The conversion gain and fundamental rejection versus input frequency at –7 dBm input power are shown in Fig. 6. The measured conversion gain is –3—8 dB and the fundamental rejection is better than 23 dB for the output frequency between 4 to 18 GHz. The transistors of the active balun are biased at 1.65 V \( V_b \) and 3 V \( V_c \), and the power consumption is 52 mW. The transistors of the doubler are all biased at 0.86 V \( V_b \) and 2 V \( V_c \), and this distributed doubler only consumes 8 mW dc power.

<table>
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<th>Table I</th>
<th>Comparison of the reported broadband active frequency doublers.</th>
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This SiGe balanced distributed doubler has broadband characteristics with a good fundamental rejection
under a lower dc power consumption compared with other balanced frequency doublers. A figure of merit

\[
\text{FOM} = \left[ 10 \log \left( \frac{100 \times P_{\text{out,2nd}}}{P_{\text{in,1st}} + P_{\text{dc}}} \right) + \text{FR} \right] \times \text{BW}
\]

is defined for frequency doublers, where \(P_{\text{out,2nd}}\) is the second harmonic output power, \(P_{\text{in,1st}}\) is the input power, \(P_{\text{dc}}\) is the dc consumption, FR is fundamental rejection and BW is 3 dB fractional bandwidth. This broadband doubler has a good FOM which is comparable to that of the InP DHBT doubler [6].

IV. CONCLUSION

A broadband balanced distributed doubler using 0.35 \(\mu\)m SiGe BiCMOS process has been developed. The sharing collector line technique is proposed to minimize the chip size.

This doubler conversion gain is better than \(-8\) dB and the fundamental rejection is better than 23 dB from 4 to 18 GHz. The dc power consumption is 60 mW, and the chip size is 1.1 \(\times\) 0.7 mm\(^2\).

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REFERENCES