A Compact 60 GHz Integrated Up-Converter Using Miniature Transformer Couplers With 5 dB Conversion Gain

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Abstract—A 60 GHz singly balanced subharmonic up-converter is presented in this letter. The monolithic microwave integrated circuit (MMIC) chip is implemented using a standard $0.13\ \mu\text{m}$ mixed-signal/radio frequency (RF) CMOS process. This circuit combines a subharmonic mixer and a three-stage cascode output amplifier. A new miniature transformer coupler is used to provide the local oscillation (LO) signals with 90° phase difference to achieve subharmonic mixing. This MMIC demonstrates a conversion gain of 5 dB for RF frequency from 58 to 66 GHz, and the 2LO-to-RF isolation is over 40 dB. The chip size is only $0.366\ \text{mm}^2$.

Index Terms—Mixer, CMOS, millimeter-wave, monolithic microwave integrated circuit (MMIC).

I. INTRODUCTION

IN recent years, there are increasing interests in the 7 GHz unlicensed bandwidth around 60 GHz due to the possibility of data communication at a rate of several gigabits. GaAs has been the dominating semiconductor material for millimeter-wave (MMW) MMICs for a long time; however, due to the improvement of the CMOS technologies and the advantages of the maturity and low integration cost, many CMOS circuits have been demonstrated in these frequency ranges [1]–[4].

Mixer is one of the key components in a millimeter-wave transceiver. A subharmonic mixer has a local oscillation (LO) frequency about half of the radio frequency (RF), which is easier to obtain than that of a fundamental mixer. Compared with a 60 GHz LO source, the 30 GHz LO source usually has higher output power, lower phase noise, and better power consumption.

In this letter, a simple sub-harmonic mixer structure is proposed. Two LO signals with 90° phase differences are provided

Fig. 1. Architecture of the mixer.

using a new 90° miniature transformer coupler. In addition, a three-stage amplifier is included at the output. This MMIC demonstrates a conversion gain of 5 dB for a RF frequency from 58 to 66 GHz and 2LO-to-RF isolation is over 40 dB with chip size of only $0.366\ \text{mm}^2$.

II. CIRCUIT DESIGN

The mixer was designed using a TSMC standard mixed-signal/RF $0.13\ \mu\text{m}$ 1P8M CMOS process. The active device (NMOS) exhibits a unity current gain frequency (f_T) of 90 GHz and a maximum oscillation frequency (f_{max}) of 106 GHz with a 1.2 V supply.

The architecture of the up-converter is shown in Fig. 1. It consists of a subharmonic mixer and a three-stage cascode output amplifier. Although Gilbert-cell mixer can also be modified for even-harmonic mixing [5], it needs more than ten devices, quadrature LO, and differential IF sources. In order to minimize the chip size of the mixer, a simple sub-harmonic mixer is proposed and shown in Fig. 1. A miniature transformer coupler is introduced to provide two LO input signals with 90° phase difference. Fig. 2 shows 3D view of this transformer coupler and Fig. 3 shows the simulated results obtained from a full-wave EM simulator (Sonnet software). To utilize the full 3-D potential of the eight metal layers, a broadside-coupled spiral structure is adopted to realize the coupler. In order to save the occupied area, the center frequency of the transformer is designed at center frequency of 50 GHz. By properly designing the gap, offset, and length of the 90° coupler to obtain the appropriate coupling, the size of it is only $85 \times 75\ \mu\text{m}^2$.

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Fig. 2. 3-D view of the 90° miniature transformer coupler.

(a)

(b)

Fig. 3. Simulated (a) magnitude and (b) phase different between S_{21} and S_{31} of the 90° transformer coupler.

Fig. 4. Chip photograph of the up-converter with a size of 0.366 mm².

The devices used in the mixer are all 36-finger NMOS devices with finger width of 2 μm . All of them are biased in satu-

Fig. 5. Measured conversion gain of the up-conversion mixer swept over LO frequency.

Fig. 6. Measured conversion gain of the up-conversion mixer swept over IF frequency.

Fig. 7. Measured conversion gain and RF output power swept over IF input power.

ration region. The IF signal feeds through a low pass filter and injects to transistor M1. By using the property of a common source transistor, the IF signals at the drain and gate of M2 have is 180° phase difference at low frequency. Therefore, the IF signals of the switching devices (M3 and M4) are out of phase. But as the frequency increases, the phase difference increases, and thus makes the IF-to-RF isolation and the conversion loss of the mixer worse. The LO signals injected to M3 and M4 are provided by the miniature transformer coupler. Two 1 pF capaci-

TABLE I
COMPARISON OF THE REPORTED SINGLE CHIP 60-GHZ TRANSMITTERS

	Conversion Gain	Output Power	DC power	Area	Technology
[1]	0.6 dB	5.6 dBm	420 mW	12 mm ²	0.15μm GaAs
[2]	37 dB	17 dBm	510 mW	6.4 mm ² (On-Chip VCO)	0.13μm SiGe
[3]	20.2 dB	15.8 dBm	281 mW	1.04 mm ² (On-Chip VCO)	0.18μm SiGe
[4]	5 dB	-2 dBm	66.9 mW	1.2 mm ² (On-Chip VCO)	0.13μm CMOS
This work	5 dB	-5 dBm	92.2 mW	0.366 mm ²	0.13μm CMOS

tors are shunted with M1 and M2 to ensure that the M3 and M4 are treated as common source transistors with respect to the LO signals. The drains of M3 and M4 are connected together, and then the fundamental IF and second harmonic LO will cancel. Finally, a three-stage amplifier is utilized to amplify the output of the RF signal. The simulated small signal gain of the amplifier is about 20 dB and a noise figure of 8 dB from 55 to 65 GHz. The simulated dc power consumption is 85 mW.

All the matching circuits of the mixer and amplifier use thin-film microstrip lines (TFMS), except the IF low pass filter. The amplifier is modified from the design reported in [6]. The matching circuit between the mixer and amplifier is simply a low impedance short stub. The sizes of the matching circuits are all very compact, and the circuit size of the amplifier is much smaller than that in [6] due to meandered TFMS. To reduce the size of the IF matching circuit, the inductor is realized utilizing helical inductors. The helical inductors have smaller sizes than those of planar spiral inductors since the turns are expanded vertically [7].

The passive circuits, including the transmission lines, capacitors, coupler and inductors, were simulated by Sonnet. The whole circuit of the up-converter was simulated by the circuit simulator (ADS). The chip photograph of the up-converter mixer is shown in Fig. 4. The chip size of the complete circuit is 0.366 mm², which is even smaller than the reported three-stage cascode amplifier in [6].

III. EXPERIMENTAL RESULTS

This circuit is measured via on-wafer probing for RF, LO, and IF ports through ground-signal-ground probes. To measure the conversion loss performance, the Agilent E8257D and Agilent 83650L signal generators are used for LO and RF sources, respectively.

The measured conversion gain swept over LO power saturates at LO power of 5 dBm at IF frequency fixed at 4 GHz with 60 GHz RF frequency. Consequently, a 5 dBm LO power is used to drive this mixer over the entire RF-frequency range. Fig. 5 shows the simulated and measured conversion gains from 20 to 36 GHz LO frequencies with IF frequency of 4 GHz. It has a measured conversion gain of better than 5 dB from 58 to 66 GHz RF frequencies. Fig. 6 shows the simulated and measured conversion gains swept IF frequency from 1 to 10 GHz with LO frequency of 28 GHz. From 2.5 to 5.5 GHz IF frequencies, the measured conversion gain is 2–5 dB. The measured conversion gain and RF output power swept over IF input power is shown in

Fig. 7, the LO and IF frequency are 28 GHz and 4 GHz, respectively. It can be observed that the RF output power is saturated at –5 dBm. The measured LO-to-RF and 2LO-to-RF isolation for RF frequency from 58 to 66 GHz are better than –40 dB and –25 dB, respectively. This mixer and amplifier employ a 1.2 and 2.4 V dc power supply as V_{DD} , respectively. The total dc power consumption of the whole circuit is 92.2 mW, but the mixer only consumes 12 mW. Table I compares the reported 60 GHz transmitters. It can be observed that this chip demonstrates a comparable performance with the smallest chip area.

IV. CONCLUSION

A CMOS up-conversion MMIC subharmonic up-converter is designed and measured for 60 GHz applications. By using a new miniature 90° transformer coupler and combining a three-stage cascode amplifier with a singly balanced mixer, this chip provides a 5 dB conversion gain from 58 to 66 GHz with a chip size of only 0.366 mm².

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