A 75-GHz Phase-Locked Loop in 90-nm CMOS Technology

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Abstract—The design and experimental verification of a 75-GHz phase-locked loop (PLL) fabricated in 90-nm CMOS technology is presented. The circuit incorporates a three-quarter wavelength oscillator to achieve high-frequency operation and a novel phase-frequency detector (PFD) based on SSB mixers to suppress the reference feedthrough. The PLL demonstrates an operation range of 320 MHz and reference sidebands of less than -72 dBc while consuming 88 mW from a 1.45-V supply.

Index Terms—Frequency divider, phase and frequency detector (PFD), phase-locked loop (PLL), reference spurs, transmission line, voltage-controlled oscillator (VCO).

I. INTRODUCTION

THE TREND for pursuing higher data rate in modern communication systems has been demonstrated in the past and will continue in the future. Recent research on 60-GHz wireless transceivers [1], [2] reveals the advantage of utilizing the 7-GHz unlicensed band and provides possible CMOS realization for the millimeter-wave front ends. Meanwhile, the wireless applications targeting even higher frequencies are also emerging gradually, such as 77-GHz anticollision systems, adaptive cruise control, and 94-GHz Doppler cloud radars. Similar situation can be found in wireline, where broadband data communications are moving toward 20 Gb/s (backplane transceivers), 40 Gb/s (optical links), and 100 Gb/s (next generation's Ethernet). These approaches all need high-speed clocks, making phase-locked loops (PLLs) continue to play critical roles in the world of communication.

As the size scales down, the CMOS devices have achieved a much higher operation frequency, which is sometimes commensurate with the speed of its bipolar counterparts. The low-power, high-integration characteristics as well as recent improvement on broadband techniques make CMOS attractive in ultra-fast PLL designs. To gain more insight into the evolution trend, we summarize the operation frequency of the fully integrated PLLs published in the literature for the past two decades (Fig. 1). It can be clearly shown that the speed of the CMOS circuits raises up by approximately three orders of magnitude, well exceeding the improvement of the device transit frequency f_T .¹ In other words, the overall progress of performance depends not only on the technology, but more importantly, the circuit technique.

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¹The f_T of 90-nm CMOS is around 100 GHz, whereas that of a 1–2- μ m device is on the order of a few GHz.

Fig. 1. Evolution of PLL circuit.

It thus inspires us to further explore the limit of the CMOS technology and design a PLL running at even higher frequency.

However, to design such an ultra-high-speed PLL implies a robust VCO together with properly arranged dividers, whose operation locking ranges need to be overlapped with each other. At such a high frequency, connecting blocks with perfect frequency alignment in a loop is much more challenging than making blocks individually. It is because any unexpected parasitic may cause significant frequency shift in the VCO or dividers, prohibiting the loop from lock. Reference spurs, on the other hand, have been another problematic issue in charge pump PLLs. The spurs are primarily due to the pulse-width comparison in the phase detectors, which translates periodic perturbation to the control line. It is well known that this issue leads to serious interferences in the adjacent channels of a wireless system.

In this paper, we present a fully integrated PLL circuit in 90-nm CMOS technology tackling these two issues. Originally designed for the 77-GHz band of automotive radars, this PLL operates at a frequency slightly lower than the desired value. The circuit uses a novel VCO design to alleviate the effective loading and achieve a high resonance frequency, and a specially designed bias circuit rejects the noise and coupling from the supply. Appropriate arrangement for different divider topologies relaxes the stringent tradeoff between operation speed and locking range. Meanwhile, a new phase and frequency detector (PFD) topology based on single-sideband (SSB) mixers is proposed to obviate the generation for pulses, leading to a truly “quiet” phase comparison and substantially suppressing the reference sidebands. To the authors’ best knowledge, it is currently the fastest fully integrated PLL for all technologies.

This paper is organized as follows. Section II describes the PLL architecture. Section III presents the design and analysis of

Fig. 2. PLL architecture.

Fig. 3. Divider arrangement. (a) Locking range normalization with presumed $2\times$ scale-up requirement. (b) Simulated locking ranges for each divider.

the building blocks, and Section IV summarizes the experiment results.

II. ARCHITECTURE

Fig. 2 shows the PLL architecture. The PLL circuit consists of a differential VCO, a divider chain with total modulus of 64, a phase and frequency detector, and a third-order loop filter. The phase locking and frequency acquisition loops are decomposed to achieve low jitter and wide operation range simultaneously. The phase and frequency detector is implemented with SSB mixers and low-pass filters to suppress the reference feedthrough. An extra divider-by-2 circuit is incorporated to provide quadrature reference inputs. Similar to that in [3], the frequency detector along with its V/I converter are automatically turned off upon lock to minimize the disturbance to the VCO. The loop filter is realized on chip to minimize the noise coupling through bonding wires. The 9-layer interconnect metals in 90-nm process provide high density fringe capacitor² [4], making the loop filter occupy only $100 \times 300 \mu\text{m}^2$.

To accommodate the severe tradeoffs between the input frequency and operation range, different types of dividers need to be employed here. Generally speaking, the injection-locked dividers [5] achieve the highest operation frequency due to the simplest structure, but usually with the narrowest locking

range. Static dividers [6], on the other hand, reveal a relatively wide range of operation, but only for low frequencies. Miller dividers [7], also known as regenerative dividers, act as a compromise between the two cases, providing reasonable locking range at moderate center frequency. As a result, a good strategy is to place the injection-locked, Miller, and static dividers in descending order of frequency as the first three stages.

Now we consider the frequency allocation of the VCO and the subsequent dividers. Based on previous design experiences, it is desirable to keep at least $2\times$ margin for PVT variations to ensure proper locking along the loop. It is because at such high frequencies, even the routing parasitics can lead to significant frequency shift. For example, a $20\text{-}\mu\text{m}$ routing path of metal4 corresponds to $1\text{--}2\text{-fF}$ parasitic capacitance, which would cause the center frequency of the first divider stage to drift by $300\text{--}500\text{ MHz}$. To ensure proper locking, we would like each divider to have a working range as wide as the VCO tuning range. As depicted in Fig. 3(a), the normalized (i.e., converted to VCO's frequency) locking range scales up by a factor of 2 as the operation frequency decreases. Simulations with different process corners and temperatures verifies this coarse yet useful estimation.

The above requirement is not very difficult to achieve if we select the dividers' topologies correctly. The Miller and static dividers actually exhibit much larger operation ranges in practice, alleviating the design requirement to some extent. Fig. 3(b) plots the simulated operation ranges for three dividers targeting 80,

²A structure containing M3–M7 produces a capacitor density of $1.6\text{ fF}/\mu\text{m}^2$.

Fig. 4. (a) Conventional LC VCO, (b) proposed realization with distributed loading.

40, and 20 GHz with injection-locked, Miller and static topologies.³ The three curves can be roughly aligned (as the bold dash line), suggesting a direct tradeoff between the input frequency and the operation range since the product of the two is approximately a constant. Note that we design and optimize the dividers for a certain input frequency first, and then exam the corresponding bandwidth. That explains why we can observe a nominally 20-GHz divider with 30-GHz operation range. Nonetheless, subtle loading adjustment and meticulous EM simulations are conducted to ensure strong locking between the VCO and dividers. It is worth noting that the third divider (i.e., the first static stage) is realized as current mode logic (CML) with “class-AB” style to speed up the operation [8]. That is, the tail currents are removed, and the switching is accomplished by gate control. The remaining three dividers at lower speed are implemented as regular CML with proper design to achieve minimum power consumption. We discuss the building blocks in detail in the following section.

III. BUILDING BLOCKS

A. VCO

The popular cross-coupled VCO serves as the most suitable candidate for ultra high-speed operation owing to its simplicity. Generally speaking, a resonator can be modeled as a short-circuited quarter-wavelength ($\lambda/4$) resonator, regardless

³The simulation is carried out with a constant input sensitivity of around 4 dBm in 90-nm CMOS.

of whether the oscillating “tube” is indeed a transmission line.⁴ Fig. 4(a) introduces a typical high-speed VCO design with a simple buffer (M_3), an injection locked divider (M_4 and $M_6 - M_7$), and a MOS varactor (M_5). The circuit oscillates at a frequency such that the corresponding wavelength is 4 times as large as the equivalent length L , leaving the ends (node A and A') as maximum swings. However, as the resonance frequency increases, the loading of the varactors, the buffers, and the dividers becomes significant as compared with that of the cross-coupled pair itself. These indispensable capacitances burden the VCO substantially. Note that none of these devices can be made arbitrarily small: $M_1 - M_2$ pair must provide sufficient negative resistance, transistor M_4 needs to inject large signal current, and M_5 has to provide enough frequency tuning. With the device dimension listed in Fig. 4(a), the circuit oscillates at only 46 GHz. Note that the device sizes have approached the required minimum and further shrinking may cause significant swing degradation.

To overcome the above difficulty, we introduce transmission lines equivalent to three-quarter wavelength ($3\lambda/4$) of a 75-GHz clock to distribute the loading and boost the oscillation frequency. As can be shown in Fig. 4(b), these lines have one end short-circuited and the other open-circuited, resonating differentially with the cross-coupled pair $M_1 - M_2$ providing negative resistance. Connecting to the one-third points of the lines (nodes A and A'), this pair forces the transmission lines to create peak swings at these nodes. The waves thus propagate

⁴Resembling the transmission line, a spiral inductor can always be approximated by a RLC model.

Fig. 5. Impedance transformation: (a) half-wavelength microstrip line, (b) rotation on Smith chart, (c) series-to-parallel conversion.

and reflect along the lines, forming the second maximum swings with opposite polarities at nodes B and B' . That is, node $A(A')$ and node $B(B')$ are 180° out of phase. As a result, the buffers, dividers, and varactors can be moved to these ends to relax the loading at nodes A and A' , making the two zenith positions bear approximately equal capacitance. With the same device dimension [M_{1-5} in Fig. 4(a)], the oscillation frequency raises up to around 75 GHz, which is a 60% improvement without any extra power dissipation.

The reader may wonder why the loading capacitance at node $B(B')$ would look differently at node $A(A')$. Indeed, the loading at nodes $A(A')$ and $B(B')$ will appear identical if the transmission line is lossless, since the $\lambda/2$ line rotates the loading impedance by exactly 360° along the outmost circle of the Smith chart. However, in a lossy line the equivalent capacitance seen from node $A(A')$ toward the load does become lower. The magnitude attenuation translates the purely capacitive loading into a lossy but smaller capacitor. Consider a typical microstrip line with $\lambda/2$ length as shown in Fig. 5(a). Made of $1\text{-}\mu\text{m}$ wide M_9 on top of M_1 ground plane, this transmission line would present a characteristic impedance (Z_0) of about $200\ \Omega$ and a quality factor (Q) of 5. Denoting the real and imaginary parts of the propagation constant as α and β , we have $Q = \beta/(2\alpha)$ and therefore $\alpha = \pi/(Q\lambda)$. The 10-fF loading capacitor (representing the capacitance of the buffer, the divider, and the varactor) locates at P_1 with a normalized impedance $z_L = 0 + j(-1.06)$. To calculate the input impedance, we rotate clockwise z_L by 360° with the radius decreasing by a factor of $\exp[-2\alpha \cdot (\lambda/2)]$:

$$\exp\left(-2\alpha \cdot \frac{\lambda}{2}\right) = \exp\left(-2 \cdot \frac{\pi}{Q\lambda} \cdot \frac{\lambda}{2}\right) = \exp\left(-\frac{\pi}{Q}\right) = 0.53. \quad (1)$$

Fig. 6. Arrangement of ground shield.

As depicted in Fig. 5(b), the new location P_2 represents the normalized impedance z_{in} which is $0.6 + j(-0.85)$. It corresponds to a 12.4 fF capacitor in series with a $120\text{-}\Omega$ resistor, which can be further translated to a parallel network (8.2 fF and $362\ \Omega$) at 75 GHz [Fig. 5(c)]. In other words, the three-quarter wavelength VCO in Fig. 4(b) experiences 18% less capacitance from $M_3 - M_5$ at a cost of higher loss, which can be compensated by the negative resistance from the cross-coupled pair. Note that the capacitance reduction becomes higher if Z_0 goes higher.

To achieve high Q and compact layout, the transmission lines are actually realized as three identical inductors in series. As illustrated in Fig. 6, two layers of ground shield made of polysilicon and metal are placed alternately underneath the spirals. Since the gaps are filled, the electric field lines are more confined between the spiral and the shield, minimizing the capacitive coupling to the substrate. Simulations including ASITIC [9] and Sonnet [10] estimate the inductor Q of the VCO to be around 16 at 75 GHz.

With the use of spiral inductors, an alternative way to explain the frequency boosting can be found by using the lumped model in Fig. 7. Here, we assume M_1 and M_{3-5} in Fig. 4 present

Fig. 7. Frequency estimation of quarter wavelength VCO with lumped model.

equivalent capacitance of $C/2$ (which is true in our design), and each inductor is denoted as L . Since nodes A and B oscillated at the same frequency, there must exist a virtual ground point x located at somewhere along the third inductor such that the Network I and Network II have the same resonance frequency ω_0 :

$$\omega_0 = \frac{1}{\sqrt{[L \parallel (2-x)L] \cdot \frac{C}{2}}} = \frac{1}{\sqrt{xL \cdot \frac{C}{2}}}. \quad (2)$$

It follows that

$$x = 0.59 \quad (3)$$

and

$$\omega_0 = \frac{1.84}{\sqrt{LC}}. \quad (4)$$

Such a first-order model implies a frequency improvement of 84%.

The above analyses also imply that, although the varactors hang on nodes B and B' , the cross-coupled pair still “sees” the loading variation at these far ends through the two-third segments of the lines. Since the resonance frequency is determined by the inductance of the first one-third segment and the overall equivalent capacitance associated with node $A(A')$, the tuning of the VCO presents monotonic increasing, similar to that of a regular LC tank VCO. Nevertheless, a standalone VCO with identical structure⁵ is developed to verify the observation. As depicted in Fig. 8(a), a monotonically increasing curve of 800 MHz is obtained across 1.2-V control voltage. In this prototype, we push the VCO frequency to the highest level, which inevitably sacrifices the tuning range to some extent. Fig. 8(b) depicts the VCO tuning over process, temperature, and supply (PVT) variations. The maximum deviation for a given control voltage is about 1.16 GHz. For a single chip experiencing 0° – 85° temperature change, the oscillation frequency shifts by 0.72 GHz. This issue implies that a more advanced technology (e.g., 65-nm CMOS) is necessary for future products operating

⁵The tuning of the VCO in the PLL is not measurable here since no pad is connected to the control line. We instead build an individual VCO with identical size but less buffer/routing loading for testing. The oscillation frequency is increased by 10 GHz as expected.

Fig. 8. (a) Measured tuning curve of a standalone 3/4 wavelength VCO (oscillation frequency is set to be 10-GHz higher than that of the VCO in the PLL), (b) simulated tuning curves for PVT variations.

at this frequency. Fig. 9 shows the simulated waveforms on different nodes of the VCO.

To suppress the coupling from power lines, the VCO is biased with a supply-independent circuit ($M_9 - M_{12}$ and R_S), as illustrated in Fig. 10(a). Here, we introduce M_{13} to absorb extra current variation caused by channel-length modulation to further reject the supply noise. That is, by proper sizing we set

$$\left| \frac{\partial I_{SS}}{\partial V_{DD}} \right| = \left| \frac{\partial I_C}{\partial V_{DD}} \right| \quad (5)$$

letting the current flowing into $M_1 - M_2$ pair remain constant [11]. Fig. 10(b) shows the currents through $M_{13}(I_C)$ and $M_{14}(I_{SS})$ as functions of supply voltage, suggesting an equal slope in the vicinity of 1.45 V. In other words, the voltage at node P is fixed, leaving the resonance frequency insensitive to supply perturbation [Fig. 10(c)]. The power penalty of M_{13} can be restrained to as low as 20–30% with proper design. The performance of this open loop compensation would slightly degrade if PVT variations occur. For example, the supply sensitivity becomes 33.3 MHz/V and -53.3 MHz/V at 1.35-V and 1.55-V supplies, respectively [Fig. 10(c)]. Nonetheless, these results are still much better than that of a conventional design without M_{13} . Note that to further reduce the noise from the current source, techniques such as [12] can be applied to this VCO.

B. Frequency Dividers

As described in Section II, the dividers are implemented as different topologies depending on the operation frequency. The first stage is realized as a simple injection-locked structure,

Fig. 9. Simulated VCO waveforms.

Fig. 10. (a) Supply independent biasing, (b) current variations, (c) oscillation frequency as a function of supply voltage.

where the natural biasing established by the cross-coupled pair of the VCO facilitates a dc coupling between the two. The complete design of the VCO, the first divider, and the buffer are shown in Fig. 11. Here, two identical injection-locked dividers are used to preserve symmetry. It produces two half-rate outputs: one goes to the second divider stage and the other to an output pad for testing. Dummy buffer is used, that along with careful layout arrives at perfect balance between the loading

at nodes B and B' . Inductor L_R is added to resonate out the parasitic capacitance associated with nodes C and C' , allowing stronger signal injection through M_5 and M_6 [7], [13].

The second divider stage is realized as a Miller divider with bandpass load, as depicted in Fig. 12(a). Similar to the second stage in [7], this structure has the output fed back to the LO port and resembles an injection-locked divider with differential input. Simulation reveals a locking range of about 11 GHz. With

Fig. 11. VCO and first divider.

the first two stages the frequency is brought down to below 20 GHz, allowing static implementation on the subsequent dividers. To extend the bandwidth without using inductors, we realize the third divider stage as class-AB structure [Fig. 12(b)]. The large instantaneous currents create high gain in the signal path and therefore higher speed. Beyond this point, the divider design becomes much more relaxed. The succeeding stages are implemented as standard static dividers with the power and bandwidth optimized.

Duo to the limited silicon area available, we are not capable of developing a full library characterizing the high-frequency models for the active and passive devices. We instead design the VCO and the first divider with the following approach. First, a preliminary version of the VCO+divider codesign based on the foundry models are taped out to estimate the accuracy of the inductors. Second, we gradually reduce the bias current of the test key until the divider fails. It allows us to obtain a coarse design margin. Since the device model below 40 GHz are well established through our previous experience on this technology, the frequency alignment of the whole divider chain could possibly be achieved in the second run. The layout skill is of great importance as well. The differential signal lines are carefully laid out with perfect symmetry so that the mismatch between the full-rate lines is less than 1 fF.

C. Phase and Frequency Detector

Ever since charge-pump topology became a mainstream in modern PLL designs, the reference clock feedthrough has been a bothering issue, especially in multi-channel applications such as frequency synthesizers. Many attempts have been made to minimize the reference spurs. For example, charge transfer technique spreads out the momentary (positive or negative) increment over longer period [14], [15]; analog phase detector utilizes current-mode logic to reduce swing [3], [16]; compensated charge-pump design balances the device mismatch [17], [18]; and distributed phase detector shortens the step of variation to avoid abrupt changes on the control voltage [19], [20]. However, none of these approaches can really get rid of the pulse generation, so the control line ripple can never be removed entirely.

To avoid producing on-off pulses which potentially create reference spurs, we perform phase detection by mixing two quadrature signals, one from the reference input (CK_{ref} , provided by the static divide-by-2 circuit) and the other from the last divider stage (CK_{div}). As illustrated in Fig. 13, an SSB mixer can distill the phase error of two synchronous signals, and reveals a sinusoidal input-output characteristic. Driven by the phase detector output V_{PD} , the V/I converter provides a continuous and proportional current, either positive or negative, to the loop filter and changes the control voltage accordingly. Since the characteristic can be approximately considered linear in the vicinity of origin and no pulse generation is involved, it achieves a truly “quiet” phase examination and reference spurs are significantly reduced. It is important to know that the current imbalance in the V/I converter is no longer an issue here, since the phase detector would create an offset between the two inputs to compensate it perfectly.

In the presence of mismatches, finite “image” would be observed at twice the PD operation frequency $2\omega_{in}$. To suppress it, a low-pass filter must be placed right after the SSB mixer. A clever realization is to load the mixer with RC networks ($R = 600 \Omega$, $C = 32$ pF) [Fig. 13(c)], which generates a corner frequency of 8.3 MHz and reject the image by more than 40 dB. Note that these low-pass filters have little impact on the overall loop bandwidth, which is designed to be around 2–3 MHz only. Fig. 14 compares the control line fluctuation of several PLLs with the same operation frequency and power dissipation but different PD topologies. The proposed structure reveals a minimum ripple of only 15 μ V, as depicted in the inset, whereas type IV and [3] induce perturbation of 13 and 4 mV, respectively.

The periodic characteristic of the phase detector implies a limited capture range. Fortunately, the frequency detection can be accomplished by introducing another SSB mixer, arriving at a wide operation range. As shown in Fig. 15, the two outputs V_{PD} and V_2 appear orthogonally in the presence of frequency error:

$$V_1 = V_{PD} = kA_1A_2 \sin(\Delta\omega_{in}t + \theta) \quad (6)$$

$$V_2 = kA_1A_2 \cos(\Delta\omega_{in}t + \theta). \quad (7)$$

Fig. 12. (a) Second and (b) third divider stages.

Here, $\Delta\omega_{in}$ represents the frequency difference between CK_{ref} and CK_{div} . Obviously, whether V_1 is leading or lagging V_2 depends on the sign of $\Delta\omega_{in}$, and it can be easily obtained by using a flip-flop to sample one signal with the other [3]. Based on the flip-flop's output, the V/I converter designated to the frequency detection loop [i.e., $(V/I)_{FD}$] injects a positive or negative current to the loop filter. This current is 3 times larger than the peak current of $(V/I)_{PD}$ to ensure a smooth frequency acquisition. To minimize the disturbance, the automatic switching-off characteristic [3] is preserved in this design by applying $\overline{ENFD}$ to $(V/I)_{FD}$ and making it disabled when the loop is locked. Similar to type IV PFD, this frequency detector can theoretically operate across an infinite range. The relatively simple structure helps to reduce the power consumption.

The very slow sinusoids V_{PD} and V_2 may cause malfunction of FF₁ if they drive the flip-flop directly, because the transitions of V_{PD} and V_2 become extremely slow when the loop is close to lock. The fluctuation caused by unwanted coupling or

additive noise would make the transitions ambiguous, possibly resulting in multiple zero crossings. To remedy this issue, hysteresis buffers are employed to sharpen the waveforms. Fig. 16 depicts the buffer design, where the cross-coupled pair $M_3 - M_4$ provides different switching thresholds for low-to-high and high-to-low transitions, and the positive feedback helps to create square waves as well. Here, $(W/L)_{1,2} = (W/L)_{3,4} = 8/0.25$, and a threshold difference of 46 mV is observed. Fig. 17 shows the complete PFD design.

IV. EXPERIMENTAL RESULTS

The PLL circuit has been fabricated in 90-nm CMOS technology and tested on a high-speed probe station with dc pads directly wire-bonded to board traces. Fig. 18(a) shows a photo of the die, which measures $1.0 \times 0.8 \text{ mm}^2$ including pads, and Fig. 18(b) illustrates the testing setup. In this prototype the reference input is provided by N4901A without any additional filters.

Fig. 13. (a) Proposed phase detector and (b) its characteristic; (c) SSB mixer with RC low-pass filter.

Fig. 14. Simulated control line voltages.

Fig. 15. Frequency detection.

The loop locks from 73.4 GHz to 73.72 GHz. The 320-MHz operation range is pretty much the VCO tuning range.⁶ Three dies are tested independently, and the frequency variations are within 50 MHz. The PLL functions properly with any supply voltage between 1.35 V and 1.55 V. The nominal power consumption

⁶Due to the limited silicon area, we do not build standalone dividers for testing.

(supply = 1.45 V) excluding output buffers is 88 mW, of which 8 mW is dissipated in the VCO, 66 mW in the divider chain, and 14 mW in the PFD and V/I converters. The reference input level can be as low as -16 dBm.

At 75 GHz, the spectrum analyzer must incorporate harmonic mixer which introduces loss of around 50 dB, resulting in a limited range on phase noise and sideband measurement. Fig. 19(a)

Fig. 16. Hysteresis buffer and its characteristic.

Fig. 17. Complete PFD design.

Fig. 18. (a) Chip micrograph. (b) Testing setup.

depicts the in-band output spectra of the VCO and the first divider under locked condition. The phase noise at 100-kHz offset measures -88 and -94 dBc/Hz, respectively. The out-of-band spectra are also shown in Fig. 19(b). Here, the heavy loss of the harmonic mixer “raise” the noise floor and make VCO phase noise invisible. The half-rate output presents a phase noise of -114 dBc/Hz at 10-MHz offset, suggesting that the VCO itself

has -108 dBc/Hz phase noise at 10-MHz offset. The sideband measurement suffers from the same difficulty. We then estimate the reference sideband as follows. First, with the highest resolution, we plot the spectrum of the output and spurs for different input amplitudes as shown in Fig. 20. By gradually turning down the input level, it can be observed that the spurs would eventually buried in the noise floor, which is 72 dB lower than the carrier,

Fig. 19. (a) In-band, (b) out-of-band output spectra of VCO and the first divider.

Fig. 20. Measurement on reference spurs.

if the reference input is less than 100 mV. Since the PLL can operate perfectly with reference input level as low as 50 mV, we conclude that the reference sidebands are less than -72 dBc.

The heavy loss of the mixers (11970W) also prohibits a direct phase noise plot of the VCO, since the spectrum analyzer E4407B requires an input of at least -50 dBm to do so. We instead depict the phase noise of the first divider's output, and compare it with the input profile as illustrated in Fig. 21. It can be shown that the two curves roughly maintain a difference of 24 dB ($= 20 \log 16$), suggesting that the PLL itself contributes negligible noise.

The time domain performance are also recorded as shown in Fig. 22. Using the reference clock as a trigger, the 75-GHz

output presents peak-to-peak and rms jitter of 609 fs,pp and 87 fs,rms, respectively, and the 37.5-GHz output reveals jitter of 2.15 ps,pp and 293 fs,rms. The difference might be attributed to the accuracy of the instruments (e.g., the harmonic mixers, sampling modules of the oscilloscope, etc.) at high speed. Nonetheless, integrating the phase noise of the 37.5-GHz output in Fig. 21 from 10 kHz to 10 MHz yields an rms jitter of 372 fs, roughly matching the measured result [21]. The loop bandwidth measures 2.5 MHz. Fig. 23 compares the reference sidebands of integer- N PLLs with similar loop bandwidth, and Table I summarizes the performance of this work and some other high-speed PLL circuits recently published in the literature.

Fig. 21. Phase noise measurement.

(a)

(b)

Fig. 22. Waveforms for (a) 75-GHz and (b) 37.5-GHz outputs.

V. CONCLUSION

A CMOS PLL with advanced millimeter-wave techniques demonstrates an operation frequency close to the device f_T . Novel VCO topology reveals significant improvement in terms of speed and noise, and the appropriate arrangement for dividers ensures locking along the loop. SSB-mixer-based PFD achieves truly quiet phase comparison, and therefore ultra low spurs. It not only provides technical solutions for present systems, but

Fig. 23. Performance comparison of reference sidebands.

TABLE I
PLL PERFORMANCE SUMMARY

	[27]	[28]	This Work
Operation Freq.	60 GHz	60 GHz	75 GHz
Multiply Ratio	1024	12	32
Phase Noise * (@ 100-kHz Offset)	-56 dBc/Hz	-95.5 dBc/Hz	-88 dBc/Hz
Clock Jitter @ 75 GHz	N/A	N/A	87 fs,rms/609 fs,pp
Clock Jitter @ 37.5 GHz			293 fs,rms/2.15 ps,pp
Supply Voltage	3 V/4.3 V	5 V	1.45 V
Power Diss.	650 mW	370 mW	88 mW
Ref. Sidebands	-50 dBc	N/A	< -72 dBc
Min. Input Level	-10 dBm	3 dBm	-16 dBm
Lock Range With Min. Input Level	3.3 GHz	150 MHz	320 MHz
Loop Bandwidth	200 kHz	178 MHz	2.5 MHz
Chip Area	1 mm x 0.8 mm	2.35 mm x 1.8 mm	1.0 mm x 0.8 mm
Technology	200-GHz SiGe	0.15- μ m GaAs	90-nm CMOS

* Reference and multiply ratio related.

also exhibits promising potential for future CMOS circuits operating beyond 100 GHz.

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