A 2.4 GHz Fully Integrated Cascode-Cascade CMOS Doherty Power Amplifier

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Abstract—This letter presents the first CMOS Doherty power amplifier (PA) fully integrated on chip. The “cascode-cascade” amplifier architecture is proposed to get rid of the bulky power splitter and facilitate the integration. The quarter wavelength transmission lines are replaced by the lumped component networks such that the whole amplifier circuit can be squeezed into the die size of $1.97 \times 1.4 \text{ mm}^2$. Fabricated in $0.18 \text{ }\mu\text{m}$ CMOS technology, the 3.3 V PA achieves 12 dB power gain. The measured output power and power added efficiency (PAE) at $P_{1 \text{ dB}}$ are more than 21 dBm and 14%, respectively. The PAE at 7 dB back-off from $P_{1 \text{ dB}}$ is above 10% and the PAE degradation is less than 29%.

Index Terms—CMOS, efficiency, fully integrated, orthogonal frequency division multiplexing (OFDM), peak-to-average power ratio (PAPR), power amplifier (PA), power back-off.

I. INTRODUCTION

WITH the thirst for high data-rate transmission, Orthogonal Frequency Division Multiplexing (OFDM) modulation technique, which is robust against multi-path fading [1], is widely used in modern high-speed wireless communication systems. However, the multi-carrier characteristic of OFDM signals leads to large peak-to-average power ratio (PAPR) and dynamic range [2]. The high PAPR results in a particular design challenge for radio frequency (RF) power amplifiers (PAs) because high power efficiency is usually achieved when PAs deliver peak power. The efficiency will degrade dramatically when RF PAs operate in back-off region. Unfortunately, the OFDM systems transmit signals at the vicinity of average power level most of the time, so the efficiency of RF PAs becomes a significant issue.

The Doherty amplifier is one of the promising solutions to enhancing power-added efficiency (PAE) in power back-off region [3], [4]. Fig. 1 shows the architecture of a classic Doherty amplifier. The main amplifier is usually biased at class AB and the auxiliary amplifier is biased at class C. In the low power region, only the main amplifier is operating because of the bias conditions. When the main amplifier is about to saturate, good efficiency can be achieved. In the high power region, the auxiliary amplifier will turn on and join power delivery. In addition,

Fig. 1. Classic Doherty PA architecture.

the combination of the auxiliary amplifier and $\lambda/4$ impedance inverter attributes to active load modulation and the main amplifier continues to increase driving current while maintaining constant voltage swing.

Conventional implementation of low gigahertz Doherty PAs requires bulky power splitters and the $\lambda/4$ transmission lines are very long. Therefore, it is not practical to develop a Doherty amplifier fully integrated on chip [5]. Several good works of Doherty PAs have been reported, but their implementations require off-chip matching networks or baluns [6]–[8]. To reduce the footprint of Doherty PAs for handheld mobile devices, miniaturization techniques have been proposed, including lumped element equivalent networks [9] and “series-type” architecture [10].

This letter presents the novel “cascode-cascade” Doherty amplifier architecture such that the bulky power splitter can be eliminated to facilitate high level of integration. The fully integrated 2.4 GHz Doherty PA was fabricated in $0.18 \text{ }\mu\text{m}$ CMOS technology. The PAE degradation of the PA at 7 dB back-off from $P_{1 \text{ dB}}$ is less than 29%. Thanks to the proposed “cascode-cascade” architecture, the CMOS Doherty PA integrates all the passive components on chip and maintains a very compact die size at the same time.

II. ARCHITECTURE AND CIRCUIT DESIGN

The proposed “cascode-cascade” Doherty amplifier architecture is shown in Fig. 2. The cascode amplifier consisting of the common-source (CS₁) and common-gate (CG) amplifiers works as the Doherty main amplifier. The cascade amplifier consisting of the common-source amplifiers CS₁ and CS₂ works as the Doherty auxiliary amplifier. The phase shift matching network in front of the CS₂ amplifier provides the functions of 90° phase shift and high impedance looking from the CS₁. Because of the high impedance, most of the power delivered by the CS₁ will be pumped into the CG amplifier. Biased at class

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Fig. 2. Proposed Doherty PA architecture.

Fig. 3. Simplified schematic diagram of the CMOS Doherty PA.

C, the CS_2 amplifier will join power delivery in high power region, just like the classic auxiliary Doherty amplifiers.

The simplified schematic diagram of the fully integrated CMOS PA is shown in Fig. 3. The cascode PA consists of the transistors M_1 and M_2 , and the cascade PA consists of the transistors M_1 and M_3 . Whereas the transistor M_2 is self-biased, the diode connected MOSFET circuits are used to bias the transistors M_1 and M_3 . In addition to establishing proper bias, the diode connected MOSFET circuits can provide a compensation mechanism for the input capacitance variation of the active devices, and, therefore, improve the linearity of the PA [11]. The size of M_3 is selected to be capable of driving twice as much output current as M_1 such that good PAE at 6 dB back-off from $P_{1\text{ dB}}$ is achieved.

Since the $\lambda/4$ transmission line at 2.4 GHz is pretty long if implemented on chip, it is replaced by the equivalent lumped element π -network as shown in Fig. 3. The $\lambda/4$ equivalent lumped-element network which consists of L_1 , L_2 , and C_1 sets up the high load impedance for the main amplifier, so the full voltage swing is reached for the high PAE at power back-off. The phase shift matching network in front of M_3 is composed of C_2 , C_3 , and L_3 . This matching network provides a 90° phase shift to synchronize the signal phases through the cascode and cascade amplifiers. In addition to phase shift, the matching network also enables the mechanism that only one-tenth of the output power from M_1 is pumped into M_3 . Most of the power from M_1 will go through the CG amplifier M_2 . Fig. 4 shows the distribution of power delivered into M_2 and M_3 .

Fig. 4. Power delivered into M_2 and M_3 .

Fig. 5. Microphotograph of the CMOS PA chip.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

The 2.4 GHz Doherty PA was fabricated with TSMC $0.18\ \mu\text{m}$ CMOS technology. The overall chip size is $1.97 \times 1.4\ \text{mm}^2$, and the chip microphotograph is shown in Fig. 5. The chip was mounted on a two-layer FR-4 board for measurement. The dc and ground pads were wire-bonded to the PCB board, and no off-chip components were needed. The supply voltage of the PA is 3.3 V.

The CMOS technology provides dual gate devices. All the transistors in the circuit are standard $0.18\ \mu\text{m}$ transistors except M_3 . The thick-oxide option is applied to M_3 for increasing its breakdown voltage and the corresponding gate length is $0.35\ \mu\text{m}$.

The measured S -parameter is shown in Fig. 6. Both the input and output return losses are better than 10 dB at 2.4 GHz. The power gain of the PA is 12 dB as shown in Fig. 7. The output power and PAE at 1 dB gain compression point are 21.5 dBm and 14%, respectively. Two peak PAE values are easily observed

Fig. 6. Measured S-parameters of the fully integrated CMOS Doherty PA.

Fig. 7. Measured power gain, output power, and PAE of the fully integrated CMOS Doherty PA.

in Fig. 7. The PAE at the power 7 dB back-off from $P_{1\text{ dB}}$ is still above 10%, and the PAE degradation is less than 29%.

IV. CONCLUSION

The “cascode-cascade” Doherty PA architecture is proposed to eliminate the bulky splitter in the conventional implementation. The 2.4 GHz fully integrated Doherty PA is fabricated in TSMC 0.18 μm CMOS technology, and the chip size is $1.97 \times 1.4 \text{ mm}^2$. The measured $P_{1\text{ dB}}$ is 21.5 dBm and the PAE degradation at 7 dB back-off from $P_{1\text{ dB}}$ is less than 29%. Thanks to the proposed architecture, the CMOS Doherty PA integrates all the passive components on chip and maintains a very compact die size at the same time.

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