Contact Resistance in Nanocrystalline Silicon Thin-Film Transistors

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Abstract—Thin-film transistors (TFTs) of nanocrystalline silicon (nc-Si:H) made by plasma-enhanced chemical vapor deposition have higher electron and hole field-effect mobilities than their amorphous counterparts. However, as the intrinsic carrier mobilities are raised, the effective carrier mobilities easily can become limited by the source/drain contact resistance. To evaluate the contact resistance, the nc-Si:H TFTs are made with a range of channel lengths. The TFTs are fabricated in a staggered top-gate bottom source/drain geometry. Both the intrinsic and the n^+ - or p^+ -doped nc-Si:H source/drain layers are deposited at 80-MHz excitation frequency at a substrate temperature of 150 °C. Transmission electron microscopy of the TFT cross section indicates that crystallites of doped nc-Si:H nucleate on top of the Cr source/drain contacts. As the film thickness increases, the crystallites coalesce, and the leaf-shaped crystal grains extend through the doped layer to the channel i layer. The contact resistance is estimated by measuring I_{DS} for several channel lengths at fixed gate and drain voltages. The results show that the contact resistance depends on the gate voltage and that the source/drain current of these TFTs at $V_{DS} = 10$ V becomes limited by the contact resistance when the channel length is less than 10 μm for n-channel and less than 25 μm for p-channel.

Index Terms—Contact resistance, nanocrystalline silicon (nc-Si:H), thin-film transistors (TFTs).

I. INTRODUCTION

INTEGRATED circuits made on organic polymer foils (plastic substrates) are under intense research and development for their desirable features of light weight, flexibility, and even deformability. However, the fabrication of circuits on organic polymer substrates usually demands process temperatures of 200 °C or less. To realize conformable transistor backplanes, electronic materials compatible with such ultralow process temperatures are needed. Nanocrystalline silicon (nc-Si:H)

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Fig. 1. Schematic cross section of the staggered top-gate bottom source/drain TFT on top of an intrinsic nc-Si:H seed layer, including layer thicknesses, materials, and functions.

is one of the candidates based on the following properties: 1) high-electron field-effect mobilities compared with a-Si:H; 2) capability of p-channel operation [1]; 3) compatibility with low process temperature; 4) compatibility with present industrial standard a-Si:H technology; and 5) insensitivity to light-induced defect generation [2]. nc-Si:H thin-film transistors (TFTs) with electron field-effect mobilities of $100 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ and higher have been reported [3]. However, as the intrinsic carrier mobilities are raised, the effective carrier mobilities easily can become limited by the source/drain contact resistance [4]. The nc-Si:H consists of a crystalline phase embedded in an amorphous matrix. If the amorphous phase lies in the current path, it may introduce undesirable source/drain contact resistance in the TFTs [5]. The properties of the crystalline phase depend strongly on the process conditions and the substrate type, and they evolve with film thickness [6], [7]. We evaluated the source/drain contact resistance of the nc-Si:H TFTs made with a range of channel lengths L by extrapolating plots of total resistance versus channel length to $L = 0$. To investigate whether the amorphous phase plays a role in determining the source/drain resistance, we studied the TFT cross sections of the channel region and of the source/drain contact regions by transmission electron microscopy (TEM).

II. EXPERIMENTS

To reduce the complexity of TFT fabrication and TEM sample preparation, all devices described in this paper are made on Corning 1737 glass substrates at a temperature that Kapton E polyimide substrates can tolerate.

The nc-Si:H TFTs are fabricated in the staggered top-gate bottom source/drain geometry on top of a nc-Si:H seed layer as shown in Fig. 1. The top gate is used to take advantage

Fig. 2. UV reflectance spectra of nc-Si:H samples with hydrogen dilution ratios of (a) 20 and (b) 30 deposited at various substrate temperatures. For easy comparison, the curves were shifted along the reflectance axis by: (a) -0.06 for 190°C , -0.03 for 150°C , and -0.09 for 120°C and (b) $+0.12$ for 150°C , $+0.04$ for 120°C , and -0.10 for 90°C .

of the highest carrier mobilities available in the nc-Si:H films. The bottom source/drain geometry is introduced to avoid the channel overetch that is usually encountered in fabricating the conventional coplanar top source/drain geometry. First an ~ 60 -nm-thick intrinsic nc-Si:H seed layer is deposited by plasma-enhanced chemical vapor deposition (PECVD), beneath the whole TFT structure, to promote rapid nucleation of the channel layer. We intentionally build the seed layer such that the crystallites do not yet coalesce. This seed layer suffices to promote crystallinity in the channel but does not conduct well electrically, with a room-temperature dark conductivity of $3.6 \times 10^{-12} \text{ S} \cdot \text{cm}^{-1}$, which avoids introducing a low shunt resistance that may produce a high OFF current. On top of the seed layer is ~ 50 -nm-thick evaporated Cr for the bottom source/drain electrodes, followed by an ~ 50 -nm-thick PECVD n^+ nc-Si:H source/drain contact layer. The source/drain patterns are defined by dry etching of the n^+ nc-Si:H layer and wet etching of the Cr layer. Then, an ~ 50 -nm-thick intrinsic nc-Si:H and an ~ 300 -nm-thick SiO_2 layer are deposited as channel and gate dielectric layers, respectively. After the contact holes are opened by wet chemical etch and dry plasma etch, an ~ 200 -nm Al layer is thermally evaporated and patterned into source, drain, and gate.

To minimize the OFF current and maximize the ON/OFF current ratio, we want the intrinsic nc-Si:H channel film to develop high crystallinity in a thin layer. The intrinsic nc-Si:H films are deposited from a gas mixture of hydrogen, silane, and dichlorosilane (DCS) at an excitation frequency of 80 MHz, an absorbed power of $86 \text{ mW}/\text{cm}^2$, and hydrogen dilution ratios of $R_i = [\text{H}_2]/[\text{SiH}_4 + \text{SiCl}_2\text{H}_2]$ ranging from 20 to 30. The very high excitation frequency ensures a good film crystallinity. The addition of 20–30 vol.% DCS to silane compensates the film from n-type to intrinsic [8]. Two bands in the ultraviolet reflectance spectra at 276 and 365 nm indicate the crystallinity of the films [9], [10]. Fig. 2 shows that films grown at higher hydrogen dilution ratio have higher crystallinity and that the crystalline volume fraction first increases and then decreases when the deposition temperature is varied from low to high at otherwise fixed deposition conditions. The room-temperature dark conductivity of an ~ 300 -nm-thick intrinsic nc-Si film deposited at 150°C is $\sim 6 \times 10^{-7} \text{ S} \cdot \text{cm}^{-1}$ for $R_i = 20$ and $\sim 3 \times 10^{-6} \text{ S} \cdot \text{cm}^{-1}$ for $R_i = 30$.

The desired properties for the n^+ - or p^+ -doped nc-Si:H layer are the following: 1) high conductivity for low source/drain contact resistance; 2) sufficient crystallinity to promote the nucleation of the channel layer in the staggered bottom source/drain TFT geometry; and 3) sufficiently thin to ensure step coverage in the following transistor fabrication. The doping of the PECVD nc-Si:H is achieved by introducing phosphine (PH_3) or diborane (B_2H_6) into the hydrogen-diluted silane source gas. The deposition parameters are a pressure of 500 mtorr, an absorbed power of $103 \text{ mW}/\text{cm}^2$, and hydrogen dilution ratios of $R_p = [\text{H}_2]/[\text{SiH}_4 + \text{B}_2\text{H}_6] = \sim 200$ for p-type and $R_n = [\text{H}_2]/[\text{SiH}_4 + \text{PH}_3] = \sim 88$ for n-type. Because the dopants are detrimental to film crystallinity, high hydrogen dilution ratios are required to obtain the nanocrystalline phase. As functions of deposition temperature at otherwise fixed deposition conditions, the sheet resistance, the room-temperature conductivity, and the dopant concentration are measured in n- and p-type nc-Si:H films. Fig. 3 shows that the highest conductivities of ~ 16 and $\sim 1 \text{ S} \cdot \text{cm}^{-1}$ are reached at the deposition temperatures of $\sim 200^\circ\text{C}$ for n-type and $\sim 150^\circ\text{C}$ for p-type, respectively. The decrease of doping efficiency at deposition temperature higher than 200°C results from the reduction of film crystallinity.

To ensure compatibility with plastic substrates, adequate crystallinity of the intrinsic nc-Si:H channel films, and sufficient conductivity of the doped nc-Si:H films, we chose the temperature of 150°C for the PECVD nc-Si:H deposition in TFT fabrication.

III. RESULTS AND DISCUSSION

A. Analysis of TFT Contact Resistance

The TFT characteristics were evaluated with an HP 4155A parameter analyzer. Because the mobility value shows a dependence on gate voltage, the effective field-effect mobility is determined by the maximum of the average slope of the transfer curve taken over the local five adjacent points versus the gate voltage. The TFTs shown in Fig. 4 have a hole field-effect mobility of $\sim 0.35 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ for channel width-to-length ratio of $W/L = 180 \mu\text{m}/30 \mu\text{m}$ and an electron field-effect mobility of $43 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ for $W/L = 160 \mu\text{m}/40 \mu\text{m}$.

Fig. 3. (a1) Sheet resistance and (a2) room-temperature conductivity and phosphorus concentration in the n-type nc-Si:H films on seed layers as functions of deposition temperature. The films were deposited from a gas mixture of $\text{SiH}_4:\text{PH}_3 = 12.5 : 1$ with a hydrogen dilution ratio of 88. (b1) Sheet resistance and (b2) room-temperature conductivity and boron concentration in the p-type nc-Si:H films on seed layers as functions of deposition temperature. The films were deposited from a gas mixture of $\text{SiH}_4:\text{B}_2\text{H}_6 = 40 : 1$ with a hydrogen dilution ratio of 200. The phosphorus and boron concentrations were obtained from the secondary ion mass spectrometry measurements. The lines are guides to the eye.

Fig. 4. Transfer characteristics of the p- and n-channel nc-Si:H TFTs fabricated at 150°C in a staggered top-gate bottom source/drain geometry. The channel dimensions are $W/L = 180\ \mu\text{m}/30\ \mu\text{m}$ for p-channel and $W/L = 160\ \mu\text{m}/40\ \mu\text{m}$ for n-channel. The TFTs have a hole mobility of $\sim 0.35\ \text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ and an electron mobility of $\sim 43\ \text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$.

When the intrinsic carrier mobilities are raised, the effective carrier mobilities may become limited by the contact resistance. The resistance can be estimated from the measurements of I_{DS} for several channel dimensions at fixed V_{DS} and V_{GS} . The total resistance from source to drain $R_{\text{TOT}} = V_{\text{DS}}/I_{\text{DS}}$ consists of the following: 1) the contact resistance R_0 , which

is inversely proportional to W , and 2) the channel resistance $R_{\text{CH}} = r_{\text{CH}} \times (L/W)$, where r_{CH} is the channel resistance per L/W . The contact resistance is determined from the intercept with the Y-axis when $R_{\text{TOT}} \times W$ (Y-axis) is plotted versus L (X-axis) and the slope denotes r_{CH} . We define a critical channel length, at which the source/drain current limitation sets in, when the contact-resistance contribution $R_0 \times W$ is equal to the channel-resistance contribution $r_{\text{CH}} \times L$. An n-channel example is shown in Fig. 5(a). We investigate the contact resistance at various gate overdrive voltages $V_{\text{GS}} - V_{\text{th}}$. Fig. 5(b) shows that the contact resistance depends on the gate overdrive voltage when the TFTs are operated at $V_{\text{DS}} = 10\ \text{V}$. In this particular case, $R_0 \times W$ decreases from 26.4×10^6 to $2.2 \times 10^6\ \Omega \cdot \mu\text{m}$ when the gate overdrive voltage increases from 5 to 20 V, and R_0 limits the source/drain current at different gate overdrive voltages when the channel length L is less than $10\ \mu\text{m}$. Fig. 6 shows a p-channel case. The considerable scatter notwithstanding $R_{\text{TOT}} \times W$ appears to depend on the channel length and suggests that the contact resistance may dominate for channels shorter than $\sim 25\ \mu\text{m}$.

B. TEM of the nc-Si:H TFTs

To investigate whether the amorphous phase in nc-Si:H affects device performance, we studied the cross sections of

Fig. 5. (a) Contact-resistance estimation for the n-channel TFTs with various channel dimensions operated at $V_{DS} = 10$ V and four gate overdrive voltages $V_{GS} - V_{th}$ using a linear fit of $(R_{TOT} \times W)$ to L . (b) Channel resistance per (L/W) r_{CH} and product of contact resistance and channel width $R_0 \times W$ at four gate overdrive voltages. All devices have source/gate and gate/drain overlaps of ~ 5 μm .

Fig. 6. Contact-resistance estimation for the p-channel TFTs using a linear fit of $(R_{TOT} \times W)$ to L . The data points are taken from transfer characteristics at $V_{DS} = 10$ V and $V_{GS} - V_{th} \approx 20$ V of TFTs with various channel dimensions. The scatter may result from uncertainty in channel dimensions or nonuniform contact resistance. All devices have source/gate and gate/drain overlaps of ~ 5 μm .

TFTs in the channel region and at the source/drain contact by TEM. Fig. 7(a) shows that the doped nc-Si:H nucleates at the Cr layer and that the leaflike crystal grain extends through the doped nc-Si:H to the channel i nc-Si:H layer. This observation suggests that the contact resistance between the doped

Fig. 7. Transmission electron micrographs at (a) the source/drain region of a p-channel nc-Si:H TFT and (b) the source/drain-gate overlap region of an n-channel nc-Si:H TFT. Undercut of the Cr at the source/drain-gate overlap is observed and is circled in (b).

nc-Si:H source/drain layer and the intrinsic nc-Si:H channel layer is not caused by the presence of a continuous amorphous layer at the doped-undoped nc-Si:H interface. Undercut of the Cr at the source/drain-gate overlap is shown in Fig. 7(b). X-ray photoemission-spectroscopy (XPS) analysis reveals that the cantilever, which is circled in Fig. 7(b), is a chromium oxide. This undercut is formed because the underlying Cr metal is etched faster by the Cr etchant than the oxidized surface of the Cr layer. Therefore, a top Cr-O slab survives the Cr etch. While the residual Cr-O cantilever might provide a possibly beneficial tapered source/drain edge, unwanted contamination may be trapped underneath it.

IV. SUMMARY

The dependence of film crystallinity on deposition temperature and the doping efficiency of PECVD nc-Si:H thin films are investigated. An electron mobility of $\sim 43 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ and a hole mobility of $\sim 0.35 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ are demonstrated in the staggered top-gate bottom source/drain nc-Si:H TFTs made at 150°C . TEM analysis indicates that the physical origin of the channel/source/drain contact resistance is not a poor interface between the channel and doped source/drain layers. Cr undercut is observed at the source/drain-gate overlap region. Analysis of current-voltage characteristics shows that the contact resistance decreases as the gate voltage increases. At $V_{DS} = 10$ V, the

source/drain current becomes limited by the contact resistance when the channel length is less than 10 μm for n-channel and less than 25 μm for p-channel nc-Si TFTs.

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