A 110-MHz 84-dB CMOS Programmable Gain Amplifier With Integrated RSSI Function

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Abstract—This paper describes a CMOS programmable gain amplifier (PGA) that maintains a 3-dB bandwidth greater than 110 MHz and can provide an 84-dB gain control range with 1-dB step resolution. The PGA can also be operated in a low-power mode with 3-dB bandwidth greater than 71 MHz. Integrated with this PGA is a CMOS successive logarithmic detecting amplifier with a ± 0.7 -dB logarithmic accuracy over an 80-dB dynamic range. It achieves -83 -dBm sensitivity and consumes 13 mA from a single 3-V supply in the normal power mode. The chip area, including pads, occupies $1.5 \times 1.5 \text{ mm}^2$.

Index Terms—CMOS analog integrated circuits, CMOS RF transceiver integrated circuits, gain-programming logic, intermediate-frequency amplifiers, IF amplifier, programmable gain amplifier, received signal strength indicator (RSSI).

I. INTRODUCTION

ALTHOUGH zero-IF and low-IF architectures have been used recently in mobile communication handsets to reduce the external component count, superheterodyne architecture, as shown in Fig. 1, continues to be widely used in many other communication systems due to its more reliable performance. Signal processing, such as amplifying or filtering, is usually realized at the IF frequency in a superheterodyne system. The circuits will consume less power if most of signal processing is performed at the IF frequency rather than at the RF frequency. Also, dc offset and flicker noise can be ignored if most of the overall system gain is realized at the IF frequency rather than at the baseband.

In wireless communication systems, the energy of the received signal spreads over a wide dynamic range after passing through unpredictable propagation paths, so a programmable gain amplifier (PGA) is usually adopted in the signal chain. In order to adjust the gain of the PGA to the optimal value suitable for subsequent processing, the received signal strength must be measured either at an intermediate frequency or at the baseband, and an automatic gain control function must be realized by feeding back the gain control signal to the PGA according to the measured received signal strength.

The voltage gain of the proposed PGA in this paper can be programmed from 0 to 84 dB in 1-dB steps, which corresponds to a programmable power gain range from -6 to 78 dB with input impedance 50Ω and output impedance 200Ω . Together with this PGA, we also designed a received signal strength indicator (RSSI) circuit in order to monitor the signal strength at the

IF frequency and to use it as an indicator of how to adjust the gain of the system. In addition, the RSSI curve will not change when we adjust the gain of the PGA. The PGA circuit we propose can be used either in the receiving path or the transmitting path, as shown in Fig. 1. In Section II, we describe the circuit architecture of the proposed PGA with RSSI. The circuit designs of the fixed gain stages and the fine gain step stage are explained in Sections III and IV, respectively. Section V describes the RSSI circuit and other related considerations. The experimental results are shown in Section VI. Finally, a conclusion is drawn in Section VII.

II. CIRCUIT ARCHITECTURE

In the design of a PGA with nonuniform gain distribution over all gain stages, as shown in Fig. 2(a) [1], accurate gain control can be easily achieved. Integrated RSSI function can also be achieved if a correction factor linked to the gain setting value is adopted. However, the RSSI calibration for different gain settings becomes very complicated when high resolution of gain control resolution is needed. Therefore, in such cases, measurement of the received signal strength needs to be performed, for example, at the baseband. But then the tracking speed of the automatic gain control loop will be lowered, and hence it is not suitable for fast fading channels. On the other hand, in a PGA with uniform gain distribution over all gain stages, as shown in Fig. 2(b) [2], the RSSI circuit can be easily attached to the PGA circuit. Unfortunately, though, the RSSI curve will not remain the same when the gain of the PGA is adjusted, and a typical family of RSSI curves is shown in Fig. 2(c) [3], [4]. In order to adjust the gain of the PGA according to the measured RSSI, a mapping from the RSSI output to the true signal level is required.

In the proposed design, shown in Fig. 3, we combine the advantages of the PGAs with nonuniform and uniform gain distribution so that excellent gain control and accurate RSSI measurement can be achieved. Furthermore in this design, the RSSI curve will not change like those of the PGA with uniform gain distribution when the gain of the whole PGA is changed. The proposed PGA circuit is composed of six fixed 12-dB gain stages, and one fine gain control PGA stage. With these six fixed gain stages, we can adjust our gain in 12-dB gain steps over a 72-dB range by selecting the input of the gain chain or one of the outputs of the six fixed gain stages, as shown in Fig. 3. Then we further increase the resolution of the whole PGA by amplifying the selected output signal through another PGA with fine gain steps, for instance 1 dB in our design, to cover the 12-dB range. In this way, the overall gain of the PGA is programmable from 0 to 84 dB with 1-dB resolution steps.

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Fig. 1. Block diagram of a typical superheterodyne system.

III. FIXED GAIN AMPLIFIER DESIGN

The gain variation of the fixed gain stages will degrade the performance of the circuit in two aspects. First, the gain setting of the PGA will change as shown in Fig. 4(a) and (b), and the resolution will be lowered. Second, the range and accuracy of the received signal level that can be detected using the RSSI will also be significantly affected, as shown in Fig. 4(c). These curves differ from those shown in Fig. 2(c) because the detector circuits are different. Some techniques, such as using matching components, i.e., N-channel input transistors with N-channel loads in a differential amplifier, can reduce gain variation. But gain control is still needed for the body effect when process variations exist. In our fixed gain stage circuit design, we use symmetric loads, as described in [8]. This kind of load can be used to reduce the common mode noise and enlarge the linear range of the load. The gain of the single fixed gain stage may vary from 6 to 15 dB, with process variations according to simulation results. In order to reduce the gain variation caused by such process variations, we designed a gain control bias circuit to generate the bias current for our fixed gain amplifiers, as shown in Fig. 5(a). The circuit will compare the actual gain of the fixed gain amplifier to an ideal gain value, which is equal to $(R_1 + 2R_2)/R_1$ and shown as line D in Fig. 5(b), and then generate the correct bias current to bias the fixed gain amplifiers. The difference between the actual output voltage V_{bn} and the ideal output bias voltage $V_{bn,ideal}$ of the operational amplifier can be shown as

$$\begin{aligned} \Delta V_{bn} &= V_{bn} - V_{bn,ideal} = g_m r_o \cdot (V_1 - V_2) \\ &= g_m r_o \{ [Av(I \cdot R_1)] - [I \cdot (R_1 + 2R_2)] \} \end{aligned} \quad (1)$$

where Av is the gain of the fixed gain amplifier, and $g_m r_o$ is the voltage gain of the operational amplifier OP in Fig. 5(a). By rearranging (1), we can obtain the gain of the fixed gain stage as

$$\begin{aligned} Av &= \frac{R_1 + 2R_2}{R_1} + \frac{\Delta V_{bn}}{g_m r_o I \cdot R_1} \\ &= Av_{set} + Av_{offset}. \end{aligned} \quad (2)$$

There is a gain offset, i.e., Av_{offset} , between the actual gain Av and the ideal gain Av_{set} , i.e., $(R_1 + 2R_2)/R_1$, but as long as the gain ($g_m r_o$) of the operational amplifier is large enough,

Fig. 2. (a) Block diagram of a PGA with nonuniform gain distribution. (b) Block diagram of a PGA with uniform gain distribution. (c) Typical family of RSSI curves of a PGA with uniform gain distribution.

Fig. 3. Block diagram of the proposed PGA.

the gain will be very close to the ideal value $(R_1 + 2R_2)/R_1$. Though the resistance variation may be rather large in a typical CMOS process, the gain will not change provided that the ratio of the resistors will remain approximately constant. Matching between the resistors is very important, and a resistor layout similar to the interdigitated layout [9] is used in this design. Since the gain control circuit operates at dc, the voltage across the resistor R_1 should not be too small as compared to the offset voltage of the replica amplifier. The voltage across the resistors $R_1 + 2R_2$ should not be too large when we consider the nonlinearity in the replica amplifier or load. In our design, we choose the typical voltage across the resistors $R_1 + 2R_2$ as 200 mV so that the load is still in the linear region under this output voltage, even if we assume that resistor variation could be 30%, and the typical voltage across R_1 is 50 mV, which means the offset voltage should be smaller than about 2.6 mV to keep the gain error of the fixed gain amplifier within ± 0.5 dB.

For the fixed gain amplifier in our design, power can be saved by lowering its bandwidth. As shown in Fig. 5(a), the loads of the fixed gain amplifiers are composed of a fixed resistor in parallel with a voltage-controlled resistor (VCR), which is in the

form of symmetric loads. The gain of the fixed gain amplifier can be shown as given by (3a)–(3c), shown at the bottom of the page, where $K = (1/2)\mu_n C_{OX}(W/L)$ and λ is the channel length modulation coefficient. In order to determine the maximum gain of the fixed gain amplifier, we can differentiate (3b) with respect to I_{tail} and it can be shown that the maximum gain occurs when the resistance of the VCR is equal to the resistance of the resistor. This means that the maximum gain occurs when the tail current is $2/(\lambda \times R_{RES})$, denoted as point B in Fig. 5(b). This gain must be larger than the gain of the fixed gain stages we choose. When the resistance R_{RES} is much lower than the resistance R_{VCR} of the VCR, the load resistance is dominated by R_{RES} , so the gain of the fixed gain amplifiers can be enhanced by increasing the tail current in (3a), shown as zone A in Fig. 5(b). Also, the 3-dB bandwidth of the amplifier is determined by the dominant pole $1/(2\pi \times R_{RES} \times C_{output})$ formed by the load resistance, i.e., R_{RES} , and the capacitance C_{output} at the output node. When R_{VCR} dominates the resistance of the load, i.e., R_{VCR} is much smaller than R_{RES} , the gain of the fixed gain amplifier can be enlarged by decreasing the tail current of the amplifier according to (3c), shown as

$$\begin{cases} A_v \cong g_{m\text{ input}} \times R_{RES} = 2\sqrt{K \frac{I_{tail}}{2}} \times R_{RES}, & R_{RES} \ll R_{VCR} & (3a) \\ A_v = g_{m\text{ input}} \times (R_{RES} // R_{VCR}) = g_{m\text{ input}} \times \left(R_{RES} // \frac{2}{\lambda I_{tail}} \right), & R_{RES} = R_{VCR} & (3b) \\ A_v \cong g_{m\text{ input}} \times R_{VCR} = 2\sqrt{K \frac{I_{tail}}{2}} \times \frac{2}{\lambda I_{tail}} = 2\sqrt{K} \sqrt{\frac{2}{I_{tail}}}, & R_{RES} \gg R_{VCR} & (3c) \end{cases}$$

Fig. 4. (a) Gain versus Gain control code when the gain of fixed gain amplifiers is larger than $A_v (= 12 \text{ dB})$. (b) Gain versus Gain control code when the gain of fixed gain amplifiers is smaller than $A_v (= 12 \text{ dB})$. (c) RSSI curves when the gain of fixed gain amplifiers is equal to, larger than, and smaller than $A_v (= 12 \text{ dB})$.

zone C in Fig. 5(b). In cases when R_{VCR} is much smaller than R_{RES} , the 3-dB bandwidth of the fixed gain amplifier is given by $1/(2\pi \times R_{VCR} \times C_{output})$. Since R_{VCR} is smaller than R_{RES} , which is a fixed value, we can expect the 3-dB bandwidth to be larger when R_{VCR} dominates the load resistance and at the same time, the current consumption is also higher. Therefore, if the IF frequency does not exceed the bandwidth of the PGA in low-power mode, then power can be saved by operating the circuit in this mode, i.e., point E in Fig. 5(b). When the IF fre-

TABLE I
SUMMARY OF GAIN SETTING OF THE FINE GAIN STEP PGA

Gain Setting	$K_3:K_4$	Gain Setting	$K_3:K_4$
0dB	18:6	4dB	18:2
1dB	18:5	5dB	18:1
2dB	18:4	6dB	18:0
3dB	18:3		

quency is higher, the circuit should be operated in high power mode, which is point F in Fig. 5(b).

IV. FINE GAIN STEP AMPLIFIER

In order to achieve fine gain step adjustment, another PGA with fine gain steps of 1 dB over a 12-dB range is arranged at the end of the signal chain. The circuit of this PGA is shown in Fig. 6. The gain step is determined by the ratio ($K = K_3/K_4$) of the gain control transistors M3 to M4 and M5 to M6. The gain of the PGA from 0 dB to 6 dB can be expressed as

$$A_{\text{PGA-1dB}} = g_{m1,2} \cdot \frac{K_3 - K_4}{K_3 + K_4} \cdot r_o. \quad (4)$$

The ratio of K_3 to K_4 , chosen for the voltage gain setting of the fine gain amplifier from 0 to 6 dB with respect to the minimum gain, is also shown in Table I. For example, the gain achieved by choosing $K_3:K_4 = 18:5$ is 1 dB larger than the gain achieved by choosing $K_3:K_4 = 18:6$. To extend the voltage gain range to cover 7 to 12 dB, we can simply apply another 6-dB PGA with the same gain setting in parallel with the former 6-dB PGA, which is also shown in Fig. 6. The change of the total width of gain control transistors M3 and M4 (M5 and M6) should be as small as possible so that the variation of the voltage at point X (point Y) does not significantly affect the g_m of the input transistors M1 and M2. If the variation of the voltage at point X (point Y) is too large, the gain step error will also increase due to the significant variation of g_m of the input transistors M1 and M2. The precision of the resolution within the 6-dB gain control range depends mainly on the factor of $((K_3 - K_4)/(K_3 + K_4))$, i.e., the matching between the switching transistors M3 and M4. Process variations and variations of environment such as temperature will affect only the gain offset, but not the resolution. We only have to take care of the mismatch between the switching transistors by using layout skills such as interdigitated arrays [9] to realize high resolutions. Besides matching between switching transistors, matching between input transistors' transconductances of the two 6-dB PGAs must be taken into consideration for the gain monotonicity of the whole PGA. The gain of the PGA from 7 to 12 dB can be expressed as

$$\begin{aligned} A_{\text{PGA-1dB}} &= \left(g_{m1,2} \cdot \frac{K_3 - K_4}{K_3 + K_4} \cdot r_o + g'_{m1,2} \cdot \frac{K'_3 - K'_4}{K'_3 + K'_4} \right) \cdot r_o \\ &= \left[g_{m1,2} \cdot \frac{K_3 - K_4}{K_3 + K_4} \cdot r_o + (g_{m1,2} \pm \Delta g_m) \cdot \frac{K'_3 - K'_4}{K'_3 + K'_4} \right] \cdot r_o \end{aligned} \quad (4a)$$

Fig. 6. Fine gain step PGA amplifier.

The coarse gain step adjusting circuit must be designed carefully to prevent reverse signal coupling from the output of the last stage of the fixed gain amplifier chain, either through the fixed gain output selecting circuit or the substrate; otherwise, the circuit may oscillate due to positive feedback. In the fixed gain output selecting circuit, coupling from gate to drain could be eliminated by cascading two stages or putting one more switch transistor between the output and the drain of the input transistor. Double guard rings are used to prevent substrate coupling in the circuit layout. Because the gain of the amplifier chain is quite high (72 dB), any circuit mismatch will cause significant offset and may even saturate the output of the amplifier chain. To avoid this, an offset cancellation scheme must be adopted. The offset cancellation circuit, shown in Fig. 8, measures the output offset level and compensates for the offset voltage by

feeding back this signal to an auxiliary amplifier accompanying the first fixed gain stage. The offset cancellation circuit can still work even if the last stage is clipping, because the input referred dc offset value will slightly change the duty cycle of the output clipping signal, and the filtered output offset value can be used for offset cancellation. This circuit is also widely used in the design of limiting amplifiers. The amplifier chain with the offset cancellation circuit will have a minimum operating frequency, and this can be set by changing g_m of the offset cancellation circuit and the capacitor. The first fixed gain stage must also be designed carefully because the auxiliary amplifier's bias current will lower the resistance of the VCR at the output of the first fixed gain stage. Thus we have to design the first fixed gain stage with a slightly higher gain to accommodate the gain reduction caused by the auxiliary amplifier.

$$\Delta I = (I_{D1} + I_{D4}) - (I_{D2} + I_{D3})$$

$$= \begin{cases} 2\frac{N-1}{N+1}I_o - 4\frac{N(N-1)K}{(N+1)^2}V_1^2 & |V_1| < \sqrt{\frac{I_o}{NK}} \\ -2(N-1)NKV_1^2 - 4NK|V_1|\sqrt{(N+1)\frac{I_o}{K}} - NV_1^2 + \frac{2NI_o}{N+1} & \sqrt{\frac{I_o}{NK}} \leq |V_1| < \sqrt{\frac{I_o}{K}} \\ 0 & |V_1| \geq \sqrt{\frac{I_o}{K}} \end{cases} \quad (5a)$$

$$= \begin{cases} 2\frac{N-1}{N+1}I_o - 4\frac{N(N-1)K}{(N+1)^2}V_1^2 & |V_1| < \sqrt{\frac{I_o}{NK}} \\ -2(N-1)NKV_1^2 - 4NK|V_1|\sqrt{(N+1)\frac{I_o}{K}} - NV_1^2 + \frac{2NI_o}{N+1} & \sqrt{\frac{I_o}{NK}} \leq |V_1| < \sqrt{\frac{I_o}{K}} \\ 0 & |V_1| \geq \sqrt{\frac{I_o}{K}} \end{cases} \quad (5b)$$

$$= \begin{cases} 2\frac{N-1}{N+1}I_o - 4\frac{N(N-1)K}{(N+1)^2}V_1^2 & |V_1| < \sqrt{\frac{I_o}{NK}} \\ -2(N-1)NKV_1^2 - 4NK|V_1|\sqrt{(N+1)\frac{I_o}{K}} - NV_1^2 + \frac{2NI_o}{N+1} & \sqrt{\frac{I_o}{NK}} \leq |V_1| < \sqrt{\frac{I_o}{K}} \\ 0 & |V_1| \geq \sqrt{\frac{I_o}{K}} \end{cases} \quad (5c)$$

Fig. 7. (a) Architecture of the RSSI circuit. (b) One of the detector circuits of the RSSI.

The output of the fixed gain stage that is chosen to be the input of the fine gain control stage has a swing ranging from 50 to 200 mV. Thus, a fixed gain stage is considered as saturated when its output exceeds 200 mV, and the rectifiers should be designed according to this operating range. However, the following saturated fixed gain stages will be used by the RSSI circuit only, but not the whole PGA signal chain, so these saturated fixed gain stages can be turned off without affecting the integrated RSSI function only if we also turn off the current of the saturated rectifiers (this is not realized in this chip), because the rectifier output current goes to zero when its input saturates. So in the presence of larger signals, we can prevent the last amplifier stages from clipping. However, this will break the loop of the offset cancellation circuit, so the offset cancellation circuit should be modified, for example, by turning on these saturated stages when the PGA is not in the operation mode in a TDMA system or using some feedback schemes like a dynamic mode feedback circuit. In another way, if we just lower the gain of the following saturated fixed gain stages, i.e., like unity gain buffers,

and still turn off the current of the saturated rectifiers, the offset cancellation circuit still maintains its function.

VI. EXPERIMENTAL RESULTS

The IF amplifier we proposed [7] has been fabricated in a 0.35- μm one-poly four-metal (1P4M) CMOS process. The capacitors used for frequency compensation in the operational amplifier for the bias circuit of the fixed gain stages are realized using MOS capacitors. The gain programming logic circuit and RSSI circuit are also integrated with the IF amplifier. The test chip is directly bonded to a PCB surrounded with the required external components. The programmable power gain range of the whole PGA is from -7.78 to 79.79 dB in normal operation mode (at 110 MHz) and -7.79 to 80.03 dB in low-power operation mode (at 71 MHz), as shown in Fig. 9. It has been found that the peaks of gain step error occur every 12 dB because of the 12-dB gain of the fixed gain stages. The gain step error is kept within ± 0.4 dB when the test chip is operated in either normal

Fig. 8. Schematics of offset cancellation circuit.

Fig. 9. IF amplifier power gain and gain error.

Fig. 11. IF amplifier OCP and IP3.

Fig. 10. RSSI output and RSSI error.

or low-power mode. The input impedance is a $50\text{-}\Omega$ external resistor across the input transistor gates, and the output impedance

is a $200\text{-}\Omega$ on chip resistor. In Fig. 10, it is shown that the measured RSSI accuracy is ± 0.7 dB, with the input signal varying from -83 to -3 dBm. The accuracy of the voltage meter used for measuring the RSSI circuit is 10 mV, which corresponds to an error of about 0.6 dB. The measured output 1-dB compression point is -4 dBV, and the third order output intercept point is 10.6 dBV, as shown in Fig. 11. The IC consumes 13 mA from 3 V when operated in normal mode and 5 mA from 3 V when operated in low-power mode. The chip micrograph is shown in Fig. 12. The chip area, including pads, occupies 1.5×1.5 mm². Table II summarizes the key measured performances and previous works.

VII. CONCLUSION

In this paper, we developed a 110-MHz 84-dB programmable gain amplifier using standard CMOS technology. Despite the process variations, excellent performance can be maintained by using the gain controlled bias circuit. The programmable gain amplifier can operate at a minimal input signal of -83 dBm.

Fig. 12. Chip micrograph.

TABLE II
SUMMARY OF CHIP PERFORMANCE AND PREVIOUS WORKS

Process	VLSI'98[10]	ISSCC'97[1]	This work (0.35 μ m CMOS 1P4M)	
	0.5 μ m CMOS	0.4 μ m CMOS	Normal mode	Low power mode
Chip size	0.4x0.6mm ²	1.2x1.35mm ²	1.5x1.5mm ²	
Gain Range	0~70dB	-17~54dB	-7.78dB ~79.79dB	-7.79dB ~80.03dB
Input noise	9nV/ $\sqrt{\text{Hz}}$	5.3nV/ $\sqrt{\text{Hz}}$	—	
Gain step	—	2dB	1dB	
Gain step error	—	-2.2 to 0.8dB	-0.4 to 0.3dB	
Input impedance	—	330 Ω resistor	50 Ω resistor	
Output impedance	—	—	200 Ω	
Supply Voltage	3.3V	3.0 $\pm$ 0.3V	3.0 $\pm$ 0.3V	
Current consumption	10mA	2mA	13mA	5mA
RSSI accuracy	Not integrated	Not integrated	$\pm$ 0.7dB	
1dB CP(out)	5dBm	-3dBm	0dBm	—
IP3(out)	20dBm(estimated)	—	14.6dBm	—
3dB Bandwidth	20MHz	120MHz*	112MHz**	74MHz**

* measured for only the last one stage of the cascaded three stages

** measured for the whole amplifier under the maximum gain setting

High gain step accuracy (± 0.4 dB) with 1-dB resolution was also achieved by this amplifier. In addition, power can be saved under the low-power mode when the IF frequency of the input signal is smaller than 74 MHz.

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