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Fabrication of diffractive optical elements using the CMOS process

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Abstract

In this paper we propose a novel diffractive optical element (DOE) which is fabricated by the conventional complementary metal-oxide semiconductor (CMOS) process. A simple post-CMOS process is employed to establish the relief pattern. The pattern can be used directly for its optical properties or can serve as a mould for subsequent replication. In this study we design a DOE with eight-phase-level gratings, which is compatible with the CMOS process. The eight-phase-level gratings have 81.4% diffraction efficiency calculated by computational and theoretical analyses. The experiment finished four-phase-level gratings.

1. Introduction

Rapid advances in diffractive optical technology have led to high performance and compact optical systems. Diffractive optical elements (DOEs) can perceptibly minimize the optical system and satisfy some particular demands more effectively than traditional optical elements. Hybrid lenses, thin lenses, wavefront correctors, wavefront generators, beam samplers and lens arrays can be improved by DOEs. Much research has fallen into three categories: design [1]; pattern generation [2]; and pattern replication [3]. The shape of the pattern should first yield high diffractive efficiency. The pattern is fabricated by various methods to satisfy the requirements. Replication is frequently used for low cost and high volume industrial production processes.

The design of DOEs should correspond to the theoretical constraints that determine the shape. The scalar theorem is usually used to predict the diffraction efficiency, but it provides only an approximate and overly optimistic solution. In contrast, the rigorous electromagnetic theorem is more precise, but complicated. The extended scalar theorem, however, adds a degree of intuition to understanding how the solutions vary, and suggests how exact solutions are calculated by commercial computer software according to the rigorous electromagnetic theorem.

The relief pattern can be performed in various ways according to the design, including grey-level masking [4],

half-tone masking [5], bulk micromachining [6], electron beam writing [7], laser beam writing and the LIGA [8] process. Table 1 summarizes the advantages of each process.

The technology for replicating DOEs has achieved high resolution. Nanometre-sized microstructures, over areas of many square centimetres, can be manufactured by casting, embossing and moulding. DOEs are most economically mass produced by replication.

Many microsensors [9–12], microactuators [13, 14] and microstructures [15–17] have been fabricated by the complementary metal-oxide semiconductor (CMOS) process. The advantage of this method is that micromachined devices can integrate with circuits in a monolithic chip [18], which reduces volume and cost.

The novel type of DOE proposed herein is adapted to the conventional CMOS process, and the scale is minimized by microfabrication. Only a simple post-CMOS process with plasma etching is required to transfer the accurate relief pattern. This pattern can be used directly for its optical properties or serve as a mould in subsequent replication. The configuration of the component and the diffractive efficiency are also presented.

2. Device design

The diffraction efficiency ultimately determines whether the DOEs will work in particular applications. The diffraction

Table 1. Various methods for fabricating DOEs.

Fabrication methods	Advantages	Process
Grey-level mask	Continuous profile and only one mask is needed	Photolithography and dry etching
Half-tone mask	Only one mask is needed	Photolithography
Bulk micromachining	Forms a special blazed angle	Wet etching
Electron beam writing	Fine features	Electron beam lithography
Laser beam writing	Fine features and cheaper equipment	Laser beam lithography
LIGA	High numerical aperture	Thermal treatment

Figure 1. First-order diffraction efficiency versus phase levels calculated by scalar theory. **Figure 2.** The shape and size of the model built in GSOLVER.

efficiency of arbitrary DOEs is directly influenced by the diffraction efficiency of the gratings. According to the scalar theory, the first-order diffraction efficiency η of an optimized N -level grating can be expressed as [1]

$$\eta = \left[\frac{\sin(\pi/N)}{\pi/N} \right]^2. \quad (1)$$

The relationship between the diffraction efficiency (η) and the phase levels (N) is thus determined and shown as the plot in figure 1, which shows that four- and eight-phase-level gratings could reach 81% and 93% diffraction efficiencies, respectively.

Four- and eight-phase-level gratings have actually been designed here, corresponding to the conventional CMOS

process. Since the conventional CMOS process is standardized and unchangeable, the essential constraint on the design of DOEs is the unequal depth of each phase level. The diffraction efficiency of the design thus cannot be merely calculated by the scalar theory, which represents the optimal case. Therefore, a real model of the design should be built and calculated.

A suitable size corresponding to the CMOS process is specified to yield high diffraction efficiency, as shown in figure 2. The model was also found by the computer software, GSOLVER, which is based on rigorous vector coupled-wave analysis and employed to analyse the various solutions. Then, the analytical equation derived from the extended scalar theory is used to verify the computational result.

Figure 3. The first-order diffraction efficiency computed by GSOLVER with various depths and wavelengths.

Figure 4. The optimum wavelength for various periods when the depth equals 5.005 μm.

In the model shown in figure 2, the eight-phase-level grating built in GSOLVER is assumed to have an index and period equal to 1.5 and 12 μm, respectively. The dashed line shows the original continuous gratings for which the brazed angle is 35.7°. The width is modified to fit the dashed line since the heights of each layer are constant and different from each other in the CMOS process. Figure 3 shows the computational result of first-order diffraction efficiency with various wavelengths of incident light, perpendicular to the substrate. The maximum diffraction efficiency is 81.4% at a 2.531 μm wavelength, and the efficiency is high enough to be useful.

According to the extended scalar theory, the optimum grating profile depth can be written as [1]

$$d = \frac{\lambda}{n - \sqrt{1 - (\lambda/T)^2}} \quad (2)$$

where d is the depth, λ is the wavelength, n is the index, and T is the period of the optimum grating profile. We let d and n equal 5.005 μm and 1.5, respectively. Figure 4 plots the value of T as a function of λ . The result is more precise over a longer period, because equation (2) is valid only for diffractive structures with very large period-to-wavelength ratios. When T and d equal

Figure 5. CMOS multi-level gratings: (a) four levels; (b) eight levels.

Figure 6. Atomic force microscopy (AFM) photographs of the CMOS four-phase-level gratings (a) before and (b) after silicon dioxide etching.

(This figure is in colour only in the electronic version)

the values of those built in GSOLVER, the derived optimum wavelength is $2.515 \mu\text{m}$, which approximates to the result, $2.5 \mu\text{m}$, computed by GSOLVER.

Summarizing this result, CMOS multi-level gratings have been proven to exhibit diffraction efficiencies up to 81.4% according to computational and theoretical analyses.

3. Fabrication

The multi-level gratings were fabricated by the conventional CMOS process and simple post-CMOS process. The fabrication follows commercial techniques and can be batch-produced immediately.

The single polysilicon three metal (SPTM) CMOS service of the Taiwan Semiconductor Manufacturing Company (TSMC) is employed to fabricate the multi-level gratings since an aluminium layer is a good etching mask for F-based plasma etching [13]. Figure 5(a) illustrates the cross section of the four-phase-level gratings. The silicon dioxide above the metal layers must be fully removed to expose those metal layers. Figure 6(a) shows the profile before the post-process, and

Figure 7. Scanning electron micrograph (SEM) of CMOS multi-level gratings.

shows metals 2 and 3 to be already exposed. The profile of metal 1 and the substrate, as shown in figure 6(b), is formed and the work is completed after silicon dioxide etching. Figure 7 shows an oblique view of multi-level gratings.

Although the four-phase-level gratings were obtained by the standard CMOS process, the diffraction efficiency is insufficient (see figure 1). The attempt to design eight-phase-level gratings was motivated by the need for higher diffraction efficiency. Figure 5(b) shows that the three metal layers, the poly, via and contact layers, are included to form the eight levels. The 'via' involves etching a tunnel in the silicon dioxide between two metal layers, such that the upper metal layer fills the via and drops down after deposition. However, the contact consists of tungsten deposited in the etching hole. The design of eight-phase-level gratings does not correspond to the CMOS rules, which require that the metal layer must be above the via or contact layers. The design still works, however, because the DOE is not an integrated circuit (IC) but an optical element. Finally, the CMOS gratings can be used directly as reflecting DOEs, or used as moulds in replication.

4. Conclusions

The four-phase-level gratings were fabricated according to the commercial CMOS process. The surface consisting of the metal layers was formed merely using silicon dioxide etching. The eight-phase-level gratings were designed for high diffraction efficiency. The criterion for the diffraction efficiency of multi-level gratings was determined and the design was shown to be extendable to other standard CMOS processes. CMOS multi-level gratings save development time and can be mass produced immediately since CMOS is a mature technology and a batch process. Furthermore, depth, alignment, dimension and shape errors can be reduced by advances in the CMOS process.

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