coefficient has been obtained by changing to the new configuration.

Conclusions: A new waveguide six-port reflectometer covering the frequency range 26-40 GHz, which makes use of a symmetrical five-port junction, has been described. In comparison with a previous design, the new configuration has been shown to be more nearly ideal, providing improvement measurement resolution as a function of frequency. Studies of further configurations based on the five-port junction are in progress.

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ANALYTICAL DELAY MODEL OF CMOS INVERTER INCLUDING CHANNEL-LENGTH MODULATION

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An analytical delay model of a CMOS inverter is introduced for the first time which includes channel-length modulation, source-drain resistance and high-field effects. Calculations of the rise, fall and delay times show good agreement with Spice simulations.

Introduction: Transient analysis of a CMOS inverter has been performed by many authors [1-6]. The models in References 1-3 were based on the Shockley MOSFET model which does not include the carrier velocity saturation effects. Therefore, these models are not suitable for applications to short-channel MOSFET circuits. Although other models (4,5) were developed with high-field effects, both the channel-length modulation effect and the parasitic source-drain resistance effect were neglected. Despite the proposal of another, better model [5], the deficiency of the linear region operation was not observed and the channel-length modulation effect was not included. Therefore, we report for the first time an analytical delay model of a CMOS inverter which considers channel-length modulation, the source-drain resistance, and high-field effects.

Model development: For the drain currents under linear and saturation operation, we incorporate our improved analytical short-channel current-voltage model [*] into the switching analysis. The MOSFET I-V model includes all second-order effects for an accurate reproduction of the static characteristics of submicrometer MOS devices. Drain current expressions are summarised as

\[ I_{DS} = \frac{-A_s + \sqrt{(A_s^2 + 4A_sI_{DS})}}{2A_s} \]

\[ V_{DS} \leq V_{DSAT} \] (1)

\[ I_{DSAT} = \frac{I_{DS}}{1 - \frac{V_{DSAT}}{V_{DS}}} \]

\[ V_{DS} > V_{DSAT} \] (2)

where \( V_{DSAT} \) is the drain saturation voltage, \( I_D \) the drain current at the onset of saturation and \( I_{DSAT} \) the channel shortening length. Details have been given elsewhere [7]. In this work the delay time \( T_d \) of a CMOS inverter is approximately defined as (fall time \( T_f \) + rise time \( T_r )/2.\) In the evaluation of delay times we focus on the discharging process of the loading capacitor under the assumption of a step input. The time consists of two intervals as follows:

\[ T_f, \] period, during which the loading capacitor voltage \( V_{L} \) drops from \( 0.9V_{DD0} \) to \( V_{DSAT} \)

\[ T_r, \] period, during which the loading capacitor voltage \( V_{L} \) drops from \( V_{DSAT} \) to \( 0\) \( V_{DD0}.\)

The differential equation which governs the behaviour of the inverter during the first period is

\[ C_{load} \frac{dV_L}{dt} + L_{DS} = 0 \]

(3)

where \( C_{load} \) is the loading capacitance. Rewriting eqn. 3, we obtain

\[ C_{load} \frac{dV_L}{dt} = -I_{DSAT} = -\frac{I_{DS}}{1 - \frac{V_{DSAT}}{V_{DS}}} \]

(4)

Integrating eqn. 4 with respect to the corresponding variable with suitable boundaries, we obtain

\[ V_{DSAT} = \int_{V_{DSAT}}^{V_{L}} \frac{1}{C_{load}} \frac{dV_L}{I_{DSAT}} \]

(5)

The second term of the left part is the contribution of channel-length modulations. By changing the integrating variable from \( V_{DSAT} \) to \( V_{DSAT} \), the integration can be carried out in a straightforward manner. As for the relationship between \( V_{L} \) and \( V_{DSAT} \), it is derived from a quasi-two-dimensional analysis for an MOSFET operated in the saturation region [7].

\[ \frac{dV_{L}}{dV_{DSAT}} = \frac{F(x) \cosh \left( \frac{V_{DSAT} - V_{DSAT} + \frac{qN_{sat}L_x}{2}}{l}\sinh \left( \frac{V_{DSAT})}{l}\right) \right)}{C_{load} \frac{dV_{DSAT}}{dt}} \]

(6)

Incorporating the relationship into eqn. 5, the final result of the left part is

\[ T_f = \frac{1}{C_{load}} \left( 0.9V_{DD0} - V_{DSAT} \right) - \frac{l}{A_s + B} \]

(7)

where \( A = F(x) \sinh x - \cosh x + x \) and \( B = 1/V_{DSAT} - V_{L} - qN_{sat} \xi \cosh x - \sinh x \) and \( 1/V_{DSAT} = \text{In} \left( \frac{V_{DSAT}}{V_{DSAT} - a_{DSAT}} \right) N \left( V_{DSAT} \right) \)

Therefore, \( T_f \) is obtained and the channel-length modulation effect is introduced into the analysis for the first time as compared to others [1-6]. As for the derivation of \( T_r \), we assume no source-drain resistance for simplicity. During this discharging interval the nMOS device is operated in the linear region and the drain current is \( I_{DSAT}. \) Substituting this current into eqn. 3, we obtain the following results:

\[ C_{load} \frac{dV_{L}}{dt} = \frac{M}{N} \left( V_{L} - V_{T} - 0.1V_{DD0} \right) - N \left( V_{DSAT} \right) \]

(8)

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where $\beta = \frac{W_{eff}}{W_{eff} + C_{o}}$, $M = V_{DD}/R_{S}$, and $N = \frac{1}{V_{DD} + V_{TH}}$. Because the fall time $T_{f}$ is given as $T_{f} = \frac{1}{\beta}$, it can be determined analytically. Applying the similar analysis to the charging process, the rise time $T_{r}$ can be obtained due to the symmetry of CMOS circuits. Therefore, we can approximately express the delay time $T_{d}$ as $(T_{f} + T_{r})/2$.

Results and conclusions: In this Section we first demonstrate the superior advantages of the I-V model used in this work over existing models. Fig. 1a and b show the simulated current-voltage characteristics of an nMOS device with $L_{eff} = 0.806 \mu m$ and $R_{d} = 0$ and $60 \Omega$ respectively. Note that $R_{d}$ denotes the total parasitic source-drain series resistance. In Fig. 1b both DC models used by the authors [4, 5] which include the carrier velocity saturation effects are also plotted. For comparison we fit these three models to $V_{DD} = 5V$ and $V_{GS} = 5V$. It is observed that much better agreement between the results of this improved model and MINIMOS 2D numerical simulations is obtained over the whole bias range than the other two models. This accuracy is due to the adequate consideration of channel-length modulations and the source-drain resistance which both become important for submicrometer MOS devices.

The calculated results of the fall, rise and delay times of a CMOS inverter plotted against the loading capacitance as a function of the source-drain resistance are presented in Fig. 2a-c, respectively, with SPICE MOS level 3 simulations. The used aspect ratio of the inverter is $W_{eff}/L_{eff} = 20 \mu m/1 \mu m$ for the pMOS and $10 \mu m/1 \mu m$ for the nMOS devices. For SPICE simulations we also insert both a source and drain resistor associated with the source and drain terminals of the nMOS and pMOS devices to account for the source-drain resistance effect. As for our proposed model it is capable of handling both the source-drain resistance and the channel-length modulation effect explicitly for the first time in the literature.

Good agreement with SPICE simulations is also obtained due to the above two important reasons. Therefore, this analytical delay model is favorable for applications of time-delay optimizations of submicrometer MOSFET circuits.

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References
Material birefringence, due to the symmetry of the structure.

Eqn. 1 can then be reduced to

$$2m(n_2^2 - n_1^2) = m_1$$  \hspace{1cm} (2)

As the mode of the waveguide is tuned by varying either \( n_0 \) or \( d \) or \( l \), the number of supported modes varies and eqn. 2 holds for a discrete number of \( m \) values.

From the results of the experiment, it can be concluded that power can be efficiently switched between the two fibres. The feasibility of such an electro-optically controlled fibre coupling switch has been demonstrated.