Effect of strain-temperature stress on MOS structure with ultra-thin gate oxide

Chia-Nan Lin, Yi-Lin Yang, Wei-Ting Chen, Shang-Chih Lin, Kai-Chieh Chuang, Jenn-Gwo Hwu *

Graduate Institute of Electronics Engineering, Department of Electrical Engineering, National Taiwan University, Room 446, Taipei 106, Taiwan, ROC

**Abstract**

A method called strain-temperature stress was adopted in this work to improve the quality of ultra-thin oxide on both MOS(p) and MOS(n) capacitors. MOS structures were baked at 100 °C under externally applied mechanical stress. Reduced gate leakage current, reduced interface trap density ($D_{it}$), and improved time-dependent-dielectric-breakdown (TDDB) characteristics were observed after tensile-temperature stress treatment without increasing the oxide thickness. On the contrary, compressive-temperature stress resulted in a degraded performance of MOS capacitors. Consequently, the tensile-temperature stress method is suggested as a possible technique to enhance the ultra-thin oxide quality of MOS structure.

**1. Introduction**

Silicon dioxide ($SiO_2$) has been used as the gate dielectric of metal-oxide-semiconductor field-effect transistors (MOSFETs) for over half a century due to its excellent stability, uniformity and simple fabrication process. As MOS devices are scaled down to the deep-submicrometer region, the thickness of $SiO_2$ should also be scaled down to achieve better performance. Based on the International Technology Roadmap for Semiconductor (ITRS), equivalent oxide thickness (EOT) should be scaled to 0.6 nm in 2013 [1]. The issue of thermal stress is of special concern as the power density increases with the scaling down of device. Since the thermal expansion coefficients between packaging material and density increases with the scaling down of device. The induced packaging materials are generally different, the mechanical stress sustained by the two different materials exists. The induced packaging-related stress may result in devices degradation, circuit malfunction and chip breakup. Device degradation due to the thermal or mechanical stress during operation is therefore of concern [2–4]. However, on the contrary, strained silicon has positive effect on channel mobility. The improvement in carrier mobility has been intensely studied by introducing strain in the channel region, such as strained-Si on SiGe substrate [5,6].

In this study, our works focus on the mechanical stress effect on MOS structures at elevated temperatures. It is well known that the atomic bonding in devices may change under external stresses such as thermal stress, mechanical stress and electrical stress. In order to simulate the situation that devices sustain mechanical and temperature stresses simultaneously, an effective method called strain-temperature stress was proposed [7]. Both the electrical characteristics of MOS structures after receiving various mechanical stresses under elevated temperatures and the effects of thermal–mechanical stress on oxide reliability were investigated.

**2. Experimental**

Both boron- and phosphorous-doped 3-inch silicon wafers with a resistivity of 1–10 Ω cm were used as the substrates of MOS capacitors. After standard RCA clean, the oxides were grown either by rapid thermal process (RTP) or anodization. The oxide thicknesses are around 25 Å for p-type and 20 Å for n-type. After front Al evaporation, capacitors with a 150 μm × 150 μm area were formed by conventional photolithography. The back oxide is then removed by using buffered oxide etchant (BOE) and then Al is evaporated as the back contact.

After the device fabrication, a quartz holder was used to strain the wafer as shown in Fig. 1a. The differences between tensile- and compressive-stress were sketched as shown in Fig. 1b and c, respectively. For strain-temperature treatments, samples with various stress conditions were baked at the temperature of 100 °C.

**3. Result and discussion**

As the strain-temperature stress was applied, both the thermal and mechanical stresses take place simultaneously. In order to make sure that the variation of electrical characteristics was caused by the strain effect, samples without any mechanical stress were baked at the same time. The $J$–$V$ curves of both p- and n-type samples baked at 150 °C were plotted as shown in Fig. 2a and b, respectively. It could be observed that there is nearly no change in the electrical characteristics.
in J–V curves even after baking at 150 °C for 30 min. As a consequence, the variations observed in the following experimental results could be considered as the influence of additional mechanical stress. In order to discuss the strain-temperature phenomenon in detail, four sections are discussed.

3.1. J–V characteristic in p-type samples

Fig. 3 shows the comparison of substrate injection current variations at 2 V for non-stress, compressive-stress and tensile-stress MOS(p) samples. After baking at 100 °C for 5 min, the devices were measured immediately and the measured data were named as “baked 1”. The devices were then stayed at room temperature for 1 week and the measured data were named as “stable 1". The stress cycle was then repeated and the data named “baked 2" and “stable 2" could be measured subsequently. For non-stress samples, it was found that the substrate injection current increased due to the thermal stress effect but got recovery after 1 week at room temperature. For tensile-stress samples, the substrate injection current in stable state is smaller than that of initial state. On the contrary, the substrate injection current increased for the compressive stressed samples. The difference in current variations could be explained by analyzing the components in substrate injection current. It is known that diffusion current (J_{diff}), depletion region generation current (J_{rg}), and surface state generation current (J_{st}) are the three main components of substrate injection current [8]. In general, J_{diff} is small when the temperature is lower than 160 °C. On the other hand, J_{rg} is stable because this component is strongly dependent on the bulk trap density in silicon. As the result, the component of J_{st}, which is strongly dependent on interface trap density (D_{it}), affects the substrate injection current in a big way. It can be concluded that the substrate injection current is strongly affected by D_{it}. In other words, the current variations might be mainly due to the changes of D_{it}. The results of calculated interface trap densities will be illustrated in section C. It is known that the lattice constants of SiO₂ and Si are different. The mismatch in lattice constant may cause a large number of dangling bonds. To re-build the atomic bonding, the Si wafer needs enough energy which may be provided by elevated temperatures. Here, we sug-

\[ a \]

\[ b \]

\[ c \]

Fig. 1. Front views of (a) strain-temperature experimental setup, (b) tensile-stress sample, and (c) compressive-stress sample.

\[ a \]

\[ b \]

\[ c \]

Fig. 2. The J–V curves of (a) MOS(p) and (b) MOS(n) samples before and after being baked at 150 °C for 30 min without stress.

\[ a \]

\[ b \]

\[ c \]

Fig. 3. Comparison of current variations for non-stress, compressive-stress, and tensile-stress MOS(p) samples.
extended because the second order lattice constants are related by stresses and elastic strains [9]. As a result, the lattice constant difference between Si and SiO2 would be reduced. As the thermal stress was applied at the same time, the dangling bonds would get energy to re-build themselves whereas the compressive-temperature stress would increase the difference of lattice constant and thus increases the $D_{it}$. It is therefore suggested that the $D_{it}$ was reduced after tensile-temperature stress but increased after compressive-temperature stress.

Fig. 4 shows the comparison of current variations for four various tensile-temperature stress conditions of MOS(p) samples. The stress value can be estimated according to the following equation [10–11].

$$\sigma = \frac{12Et}{4a^2 - 3t^2}$$  \hspace{1cm} (1)

where $E$ is the Young’s modulus ($E = 130$ GPa for (100) silicon orientation), $y$ is the total thickness of the bending stacks ($y = 1.52 \times 10^{-3}$ m for the bending stacks), $t$ is the total thickness of the wafer ($t = 3.8 \times 10^{-4}$ m), $L$ is the diameter of the wafer ($L = 7.62 \times 10^{-2}$ m) and $a$ is equal to $L/4$. The stress values for light, moderate, and strong tensile-stress are 42.3, 56.4, and 70.5 MPa, respectively. For the long-time tensile-stress sample, it was stressed with 56.4 MPa and baked for 30 min while the others were baked for 5 min. It shows that the device under strong tensile-stress reveals better Si/SiO2 interface quality than the moderate and light tensile stressed samples. On the other hand, although the long-time tensile-stress sample was stressed with moderate stress value, it exhibits the best Si/SiO2 interface quality. In short, both applying larger tensile-stress or increasing the baking time could improve the interface quality.

3.2. J–V characteristic in n-type samples

In addition to MOS(p) samples, it is interesting to discover the effects of strain-temperature stress on MOS(n) samples. From the prior experimental results, it is known that tensile-temperature stress enhances the performance of ultra-thin oxide, and the long-time tensile-stress shows the best improvement in comparison with the others. Therefore, the long-time tensile-stress was utilized in this experiment.

The cumulative distributions of gate current density for anodization (ANO) oxides and rapid thermal oxidation (RTO) oxides were shown in Fig. 5 and Fig. 6, respectively. The insets of Fig. 5 and Fig. 6 show the typical $J$–$V$ curves of MOS(n) sample before and after tensile-temperature stress treatment. For the RTO MOS(n) devices, just like the MOS(p) devices, the gate injection currents are almost the same before and after tensile-temperature stress treatment. On the contrary, the gate injection currents reduced apparently in the ANO MOS(n) devices as shown in Fig. 5. It is supposed that during the anodization process the negative ions were attracted to the wafer by the positive electric field and thus would create hidden defects in the oxide. The hidden defects might introduce the increase in gate leakage current. As the tensile-temperature stress was applied, the above defects would be eliminated thus reduces the gate injection current density. However, for both the RTO and ANO samples, an apparent reduction in substrate injection current due to tensile-temperature stress could be observed. The results are also believed due to the improvement in interface performance as stated above.

3.3. Extracted $D_{it}$ for both n- and p-type devices

The extracted $D_{it}$ at flatband condition of RTO oxides for both MOS(p) and MOS(n) devices before and after tensile-temperature stress treatment were plotted in Fig. 7. The $D_{it}$ is extracted by using
two frequencies $C-V$ method [12], and the frequencies used here were 1 M and 10 kHz. For both MOS(p) and MOS(n) devices, it could be observed that $D_{it}$ reduces apparently after the tensile-temperature stress treatment. This observation is consistent with the prior suggestion that the tensile-temperature stress would re-build the dangling bonds at Si/SiO$_2$ interface and therefore reduce the $D_{it}$.

3.4. Reliability of p-type strain-temperature stressed samples

Fig. 8 and Fig. 9 show the cumulative failure distribution of time-to-breakdown $t_{\text{BD}}$ for compressive-temperature, tensile-temperature, and control MOS(p) samples under constant voltage ($-17.6$ MV/cm) stress and constant current ($-300$ A/cm$^2$) stress, respectively. As the stress was applied, the electrons gain enough kinetic energy and incur collisions with atoms in oxides thus induce the traps. The increased traps may connect to a leaky path and then eventually cause the oxide breakdown. As the gate oxide breakdowns, the gate current increases and the gate field decreases abruptly. The inset of Fig. 8 reveals that the tensile-temperature stressed sample presents the best ability to prevent breakdown, while the compressive-temperature stressed sample exhibits the worst. In the same way, the inset of Fig. 9 also shows that the tensile-temperature stressed sample performs the best reliability in constant current $t_{\text{BD}}$ characteristics. Moreover, both the variations in the insets of Fig. 5 and Fig. 6 show barrier lowering which can be accounted for effective hole trapping. Also, it could be observed that the effective hole traps generated in tensile-temperature stressed sample are less than those in control and compressive-temperature stressed samples. It is known that the breakdown characteristics are related to interfacial property and trapping behavior [13–15]. Both the mechanisms, such as filling of intrinsic traps and stress-induced traps generation, had been proposed to explain the oxide degradation during high field stressing. The interface trap generation is strongly related to the Si/SiO$_2$ interfacial bonding as well. The accelerated electrons can break the weak bonds and cause damage at the interfaces. Since the tensile-temperature stress treatment is suggested to be able to enhance the interfacial bonding and reduce $D_{it}$, it is rational to observe that the tensile-temperature samples demonstrate improved interfacial property. The stronger interfacial strained bonds in tensile-temperature stressed samples prevent the damage from hot electrons and reinforce the breakdown endurance. In addition, the improvement of MOS(n) in time-zero dielectric reliability tests is also observed. It is effective in improving the oxide reliability by utilizing tensile-temperature stress.

4. Conclusion

In this work, the effect of strain-temperature stress on MOS structure is explored. The experimental results show that the tensile-temperature stressed devices exhibit the improved performance in electrical characteristics with respect to compressive and control samples. The tensile-temperature stressed oxides exhibit not only the reduced substrate injection current but also the improved endurance of breakdown. It is believed that samples after packaging and operated under certain temperature should sustain strain-temperature effect inevitably. The effect of strain-temperature stress is important to MOS capacitors with ultra-thin oxides.

Acknowledgement

The authors want to thank the National Science Council, ROC, for supporting this work under Contract No. NSC 96-2628-E-002-246-MY3.
References