The trap charge at the Si(P)–SiO$_2$ interface was studied using the bias–temperature aging technique. The formation of the interface trap charge at the Si–SiO$_2$ interface is attributed to the mobile ion inside the oxide. The peak in the interface trap density distribution can be produced or eliminated by bias–temperature treatment and appears to be dependent on the preparation conditions.

1. INTRODUCTION

Bias–temperature aging of a metal/oxide/semiconductor (MOS) capacitor is one of the methods used to characterize the oxide properties. The motion of ions inside the oxide$^1$, the interface trap charge $Q_{it}$ (ref. 2), the effect of annealing on the interface trap charge$^3$, the effect of ionizing radiation on the interface states$^4$ and the effect of radiation on the interface trap density$^5$ can be studied by observing the change in the capacitance–voltage ($C–V$) curves produced by aging.

We utilized this technique to investigate the surface trap at the p-Si–SiO$_2$ interface during test runs in our laboratory. There are many reports regarding the origin of the interface trap. It can be caused by dangling bonds$^6$, strained bonds$^7$ or impurity ions such as Na$^+$, K$^+$, Li$^+$ etc.$^8$ In this paper we shall report the results of our investigations of the interface trap which are different from those reported earlier. The location of the interface trap peak in the silicon energy gap appears to depend on the preparation conditions and the thickness of the oxide. The interface trap peak can be produced by treatment in electric fields at elevated temperatures, and can be erased by repeating this treatment with the electric field in the opposite direction. The same phenomenon was also observed in wafers which had been prepared in another institution.

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2. SAMPLE PREPARATION

A (100)-oriented p-type silicon wafer with a resistivity of 3 Ω cm was used as the substrate of the MOS capacitor. The wafer was cleaned first in a trichloroethylene (TCE) solution in an ultrasonic cleaner for 5 min and then in acetone. The wafer was rinsed with deionized (DI) water and was then etched with a hydrofluoric acid buffer solution (30 cm³ H₂O, 10 cm³ hydrofluoric acid and 20 g NH₄F) to remove the oxide from the wafer. After this etching the wafer was rinsed thoroughly in DI water and boiled for 10 min first in a TCE solution and then in an acetone solution. After boiling in the acetone solution, the wafer was rinsed in DI water and was subsequently heated in an 8:1 H₂SO₄:HNO₃ solution for 10 min at a temperature of 50 °C and again rinsed in DI water. Finally, the wafer was etched with a buffered hydrofluoric acid solution and then rinsed in DI water. Dry oxidation was carried out at 1000 °C in a conventional diffusion furnace. Aluminium was then evaporated onto the oxide to form the MOS capacitor electrode. The contact was a circle of diameter 8 × 10⁻³ in. Similarly, aluminium was evaporated onto the back side of the silicon wafer after the oxide had been etched away.

The $C-V$ characteristics of the MOS capacitor were then measured. The capacitor was first biased for a few minutes with a d.c. voltage of 20 V with the gate negative with respect to the silicon substrate and was then annealed in a nitrogen environment at a temperature of 400 °C for 5 min. The high frequency $C-V$ curve of the capacitor is shown in Fig. 1, curve 1. As the bias voltage is increased in the positive direction, a series of curves is obtained as indicated in Fig. 1. It can be seen that the $C-V$ curves shift horizontally to the left as the voltage increases. When the voltage exceeds 3 V, the horizontal shift is accompanied by a distortion of the lower
portion of the $C-V$ curve. The distorted region becomes insensitive to further increases in the bias voltage. The shift in the $C-V$ curve is a reversible process as curve 1 can be recovered by applying $-20$ V to the gate and then annealing at $400 \, ^\circ C$ in a nitrogen environment.

3. ANALYSIS

The interface trap density $D_{it}$ is defined as

$$D_{it} = \frac{1}{q} \frac{dQ_{it}}{d\Psi_s} \text{ cm}^{-2} \text{ eV}^{-1}$$  (1)

where $Q_{it}$ is the interface trap charge per unit area and $\Psi_s$ is the surface potential. The gate voltage $V_g$ is the sum of the voltage drop $V_{ox}$ across the oxide, the surface potential and the difference $\Phi_{ms}$ between the work functions of the metal and the semiconductor:

$$V_g = V_{ox} + \Psi_s + \Phi_{ms}$$  (2)

$V_{ox}$ can be found from the total charge at the Si–SiO$_2$ interface and is given by

$$V_{ox} = \frac{Q_{it} + Q_s}{C_{ox}}$$  (3)

Therefore $D_{it}$ can be found from the expression

$$D_{it} = \frac{C_{ox}}{q} \frac{d}{d\Psi_s} (V_g - V_{gth})$$  (4)

where $V_{gth}$ is the gate voltage in the absence of the interface trap charge. Figure 2

![Graph showing $D_{it}$ distribution after biasing at various voltages followed by heat treatment (oxide thickness, 660 Å): curve 1, -20 V; curve 2, +1 V; curve 3, +3 V; curve 4, +5 V; curve 5, +10 V; curve 6, +15 V; curve 7, +20 V.](image)
shows the $D_{it}$ distribution for the $C-V$ curves shown in Fig. 1. There is a peak in the distribution at $E-E_i = -0.12 \text{ eV}$ and its magnitude increases with the voltage applied to the gate. Figure 3 shows the $D_{it}$ distribution for the MOS capacitor as a function of the oxide thickness. It can be seen that the location of the peak depends on the oxide thickness.

![Image](image_url)

Fig. 3. $D_{it}$ distribution for various oxide thicknesses (bias voltage, +5 V): curve 1, 470 Å; curve 2, 525 Å; curve 3, 660 Å; curve 4, 780 Å; curve 5, 800 Å; curve 6, 950 Å; curve 7, 1220 Å.

The effective mobile charge $N$ can be found from the equation

$$N = C_{ox} \frac{\Delta V_{FB}}{q}$$

where $\Delta V_{FB}$ is the shift in flat-band voltage with respect to Fig. 1, curve 1, and $C_{ox}$ is the capacitance of the oxide per unit area. The total interface trap charge can be found by integrating $D_{it}$ over the energy levels in the energy gap. Figure 4 shows the relationship between the effective mobile charge and the total interface trap charge with respect to Fig. 2, curve 1, for the energy levels at $-0.35 \text{ eV}$ and $0.3 \text{ eV}$. As can be seen from the figure, the interface trap charge increases with the mobile charge.

4. DISCUSSION AND CONCLUSION

We have compared the optical responses of capacitors with and without distorted $C-V$ curves. Figures 5 and 6 show the optical responses of the $C-V$ curves for capacitors illuminated by a light bulb. After negative bias–temperature treatment both capacitors show the theoretical low frequency effect under illumination (Figs. 5 and 6, curves 1). However, after positive bias–temperature treatment the capacitor with the distorted $C-V$ curve is light sensitive in the lower
Fig. 4. Relationship between the mobile charge and the interface trap density for films of thickness 525 Å (×) and 660 Å (○).

Fig. 5. Distorted $C-V$ curves under illumination (oxide thickness, 660 Å): curve 1, negative bias; curve 2, positive bias.

distorted region (Fig. 5), whereas the undistorted capacitor is light sensitive in the upper region (Fig. 6). In both cases the behaviour shows that the interface trap density is increased after positive bias–temperature treatment because the decrease in the interface trap response time under illumination makes the trap capable of following the high frequency signal and therefore causes the total capacitance to approach the oxide capacitance.
The direction of the shift in the $C-V$ curve is consistent with the interpretation that it is due to the motion of mobile ions in the oxide. The peak in the $D_{it}$ distribution occurs when the capacitor is annealed at 400 °C in a nitrogen atmosphere after positive biasing for a few minutes. It is not necessary for the annealing to be performed in a nitrogen environment. As indicated in Fig. 4 there is a correlation between the interface trap density and the mobile ion charge. We have also investigated the effect of annealing the capacitor in a hydrogen atmosphere at 400 °C. No significant change was observed in the $D_{it}$ distribution. This indicates that the interface traps are not due to broken bonds. We have also illuminated the capacitor with UV light after applying a voltage to the gate. Again, no significant change in the peak in the $D_{it}$ distribution was observed.

The location of the peak in the energy gap generally differs from wafer to wafer. Figure 3 suggests that the location of the peak depends on the oxide thickness. However, we are not sure whether the same peak location could be reproduced in a capacitor with the same oxide thickness. We have also examined wafers processed in another laboratory and have observed similar behaviour in $D_{it}$.

As reported in this study the interface traps can be attributed to the mobile ions inside the oxide. However, we are not sure what species is involved. The peak in the interface trap distribution depends on the preparation conditions. It can only be produced or removed by the application of a voltage to the gate followed by heat treatment. The effects of the preparation conditions on the interface trap distribution and the mechanism of the formation of peaks in the distribution as a result of heat treatment are still under investigation.
REFERENCES