81.5–85.9 GHz injection-locked frequency divider in 65 nm CMOS

L.-C. Cho, K.-H. Tsai, C.-C. Hung and S.-I. Liu

An injection-locked frequency divider (ILFD) using the shunt-series inductive peaking technique is proposed. Fabricated in a 65 nm process, the proposed ILFD and a conventional one have the measured locking range of 81.5–85.9 and 71–77.4 GHz, respectively. Compared with the conventional ILFD, the measured free-running frequency of the proposed one is increased by 12.5%. Both ILFDs have core area of 0.036 mm² and power of 12 mW for a 1.55 V supply without buffers.

Introduction: Frequency dividers are widely used in frequency synthesizers and phase-locked loops. The injection-locked frequency divider (ILFD) [1–4] is attractive because of high operation frequency and low power consumption. The conventional ILFD is realised by an LC-tank oscillator with an injection input [1]. To maximise the operation frequency of an ILFD, the shunt-series inductive peaking technique [5] is adopted in the proposed ILFD. The conventional ILFD and the proposed one are realised in a 65 nm CMOS process by using the same active and passive devices with the same power and area. Experimental results demonstrate that the measured free-running frequency of the proposed ILFD is increased by 12.5%.

Circuit description: For a conventional ILFD [1], it is composed of an LC-tank oscillator and an injection transistor. Its output frequency is given as \( f_{L} = 1/\sqrt{LC} \) where \( L \) is the inductor and \( C \) is the total equivalent capacitance of the LC tank. To have a higher output frequency, the proposed ILFD is as shown in Fig. 1a. The inductors are split and the cross-coupled pair is appropriately reconnected. It is similar to the shunt-series inductive peaking technique in [5]. To analyse the locking range of the proposed ILFD, its differential equivalent circuit is as shown in Fig. 1b where \( C_1 \) is the total grounded capacitance at the nodes \( V^+ \) and \( V^- \) and \( C_2 \) is the total grounded capacitance at the nodes \( V_{gM4} \) and \( V_{gMS} \). The shunt inductors \( L_2 \) and the series inductors \( L_1 \) realise the shunt-series peaking technique [5]. Similar to [6], when the ILFD is locked, the injection current \( I_{in} \) is decomposed into the in-phase and quadrature components as

\[
I_{in} = I_q(\phi) \cos(\omega t + \phi) + I_i(\phi) \sin(\omega t + \phi)
\]

Let the drain and source voltages of the injection transistor \( M_3 \) be defined as

\[
V_{DS} = V_i \cos(\omega t + \phi) \quad \text{and} \quad V_{DS} = -V_i \cos(\omega t + \phi)
\]

The input impedance in Fig. 1b is expressed as

\[
Z_{in}(S) = \frac{2sL_2 \left( \frac{2sL_1}{Z_{eq}} + 1 \right) + 2s^2L_1L_2C_1}{S^4L_1L_2C_1C_2 + \frac{2S^2L_1L_2C_2}{Z_{eq}} + \frac{s^2L_1C_2}{L} + I_L} + \frac{2sL_1 + L_2}{Z_{eq}} + 1
\]

where \( Z_{eq} \) is the impedance of the injection transistor \( M_3 \). To simplify the analysis, assume \( L_1 = L_2 = L/2 \), \( C_1 = C/2 \) and \( C_2 = C/2 \). Neglecting the injection transistor \( M_1 \) and the injection current \( I_{in} \), the output resonant frequency of the proposed ILFD is calculated as

\[
\omega_0 = \sqrt{\frac{6 - 2sL_2}{LC}}
\]

Compared with the conventional ILFD [1], the output resonant frequency of the proposed one is increased by 23.6%. Once the input frequency of the injection transistor \( M_3 \) varies, the in-phase and quadrature frequency of the proposed one is increased by 23.6%. Fig. 4 shows the measured locking range denoted by \( \Delta \omega_{lock} \) is estimated as

\[
\Delta \omega_{lock} = 2(\omega_{max} - \omega_{min}) = \frac{4g_{eqM3}}{C}
\]

From (4) and (8), this ILFD improves the output frequency and locking range.

Experimental results: The proposed ILFD and the conventional one have been fabricated in 65 nm CMOS process. Fig. 2 shows the die photos. These two ILFDs have the same active devices and inductors. So they have the same area and power consumption. Each ILFD has core area of 0.036 mm² and power of 12 mW for a 1.55 V supply without buffers. The input frequencies of 85.9 GHz, the measured phase noise is –88.5 dBc/Hz at 500 kHz offset frequency. Table 1 summarises the performance of the frequency divider compared with the previous works.
Conclusion: A shunt-series peaking ILFD and a conventional one have been fabricated in a 65 nm CMOS technology. The equivalent circuit of the proposed ILFD is given and the analysis results are presented. Compared with the conventional ILFD, the measured free-running frequency of the proposed one is increased by 12.5%. Both the analysis and the experimental results are given to demonstrate the proposed circuit.

Acknowledgment: The authors thank UMC Inc. and Media-Tek Inc. for chip fabrication and NSC for support.

References

Table 1: Summary and comparison

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<tbody>
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<td>Technology</td>
<td>0.13 µm CMOS</td>
<td>65 nm CMOS</td>
<td>90 nm CMOS</td>
<td>65 nm CMOS</td>
<td>0.13 µm CMOS</td>
<td>65 nm CMOS</td>
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<tr>
<td>Centre frequency (GHz)</td>
<td>50–55</td>
<td>90 GHz</td>
<td>102 GHz</td>
<td>101.3 GHz</td>
<td>71.2 GHz</td>
<td>76 GHz</td>
<td>85.5 GHz</td>
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<td>Dividing range (GHz)</td>
<td>50.31–50.39</td>
<td>82–94</td>
<td>99–105</td>
<td>102–105.1</td>
<td>6.4–7.8</td>
<td>71–77.4</td>
<td>81.5–85.9</td>
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<td>Locking range (GHz)</td>
<td>0.08 (0.1%)</td>
<td>12 (13.6%)</td>
<td>8 (5.8%)</td>
<td>15.6 (13.7%)</td>
<td>9.6 (13.6%)</td>
<td>6.4 (8.4%)</td>
<td>4.4 (5.7%)</td>
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<td>Supply (V)</td>
<td>1.5</td>
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<td>Power (mW)</td>
<td>3</td>
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<td>3.3</td>
<td>5.5</td>
<td>4.4</td>
<td>12</td>
<td>12</td>
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<tr>
<td>FOM (GHz/mW)</td>
<td>0.026</td>
<td>3.06</td>
<td>1.82</td>
<td>2.04</td>
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<td>Area (mm²)</td>
<td>0.49 × 0.47</td>
<td>1.15 × 0.85</td>
<td>0.66 × 0.51</td>
<td>0.2 × 0.18**</td>
<td>None</td>
<td>0.2 × 0.18**</td>
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*Input power 15 dBm, **FOM = locking range/power, ***core circuit only*