Fast-Switching Frequency Synthesizer with a Discriminator-Aided Phase Detector

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Abstract—A phase-locked loop (PLL) with a fast-locked discriminator-aided phase detector (DAPD) is presented. Compared with the conventional phase detector (PD), the proposed fast-locked PD reduces the PLL pull-in time and enhances the switching speed, while maintaining better noise bandwidth. The synthesizer has been implemented in a 0.35-μm CMOS process, and the output phase noise is −99 dBc/Hz at 100-kHz offset. Under the supply voltage of 3.3 V, its power consumption is 120 mW.

Index Terms—Bandwidth adjusting, fast acquisition, fast locking, frequency synthesizers, phase detectors, phase-locked loops.

I. INTRODUCTION

PHASE-LOCKED loop (PLL) circuits have been found to be useful whenever there is a need to synchronize a local oscillator with an independent incoming signal, such as serial data links and RF wireless communications. In order to optimize the loop performance, some features should be taken care of [1], [2]. First, to minimize output phase jitter due to external noise, the loop bandwidth should be made as narrow as possible. Second, to minimize output jitter due to internal oscillator noise, or to obtain best tracking and acquisition properties, the loop bandwidth should be made as wide as possible. These principles obviously oppose each other; and therefore some compromises between these two principles are always inevitable. The block diagram of a PLL with a discriminator-aided phase detector (DAPD) is shown in Fig. 1. One could leave the discriminator connected permanently and/or merely weight the relative contributions of the system so as to obtain the desired damping. The discriminator-aided path adds to lock the PLL quickly. Once the PLL is in lock, a better bandwidth can be maintained while the discriminator is disconnected.

In this paper, a novel DAPD is presented to reduce pull-in time \( T_p \) and to enhance the switching speed of the PLL, while maintaining the same noise bandwidth and avoiding modulation damping. Section II describes the basic concept of the proposed structure. Sections III and IV present the realization and the measurement of the system, respectively, and Section V concludes the paper.

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II. BASIC IDEA AND MODEL

A simple charge-pump PLL consists of four major blocks: the phase detector (PD), the charge-pump circuit, the loop filter, and the voltage-controlled oscillator (VCO) [3]–[6]. Fig. 2 shows the linear model of a charge-pump PLL-based frequency synthesizer. The closed-loop transfer function can be represented as

\[
H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{2\pi \cdot N \cdot K_{PD} \cdot Z_{LF}(s) \cdot K_{VCO}}{sN + 2\pi \cdot K_{PD} \cdot Z_{LF}(s) \cdot K_{VCO}}.
\]

The conventional PD is implemented in conjunction with a charge-pump loop filter in the PLL, as illustrated in Fig. 3. To determine the transfer function of the PD, assume there is a time interval \( \tau \) between two input signals \( R \) and \( V \) in the PD, the output current of the charge-pump circuit is a pulse of duration \( \tau \), and the amplitude of the charge-pump current is \( I_{F0} \). In the continuous-time approximation, the average value \( \bar{I}_P \) per input signal period \( T \) can be given as

\[
\bar{I}_P = \frac{Q}{T} = I_{F0} \cdot \frac{\tau}{T} = \frac{I_{F0}}{2\pi} \cdot \theta_e.
\]

The transfer function curve of a linear PD is shown in Fig. 4(a), where the vertical axis represents the charge injected into the loop filter during one period of the input signal. The characteristic of a nonlinear PD, as shown in Fig. 4(b), can be divided into two regions [7]. It has the same characteristic within the locked-in region as that of the linear PD, but the acquisition time will be reduced with the steeper characteristic outside the locked-in region. When designing a PLL with the nonlinear PD, first the central slope is determined to fulfill the requirement of noise and modulation for the PLL with a standard PD. Then, the slope near \( \theta_e = \theta_{AD} \) is gradually increased to improve acquisition speed. The proposed nonlinear PD can be built with delay cells and standard PD circuits, as shown in Fig. 4(c). The standard PD is a digital circuit, triggered by the positive edge of the input reference signal \( R \) and the output feedback signal \( V \). Considering the delay cells with \( \theta_{AD} \), the PDs decide the position of the phase difference \( \theta_e \) among these regions. According to the value of \( \theta_e \), the charge pump will output the corresponding current controlled by the up signals \( U \) or the down signals \( D \). The behavior model of the nonlinear PD can be explained by the waveforms of Fig. 4(d). According to the time difference between both input signals \( V_r \) and \( V_o \), the up signals \( U \) are used to increase and the down signals \( D \) are used to decrease the frequency of signal \( V_o \). The nonlinear PD always generates the right signal to equalize the frequency of both input signals as the conventional PD. The time interval \( \tau \) is positive.
Fig. 1. Block diagram of PLL with discriminator-aided phase acquisition.

Fig. 2. Linear model of PLL frequency synthesizer.

Fig. 3. Phase detector with charge-pump filter.

(negative) where $V_i$ leads (lags) $V_o$. When $\tau$ is larger than $\tau_{AD}$ ($=2\pi\theta_{AD}$), $U_{AD}$ may appear “high” level; when $\tau$ is smaller than $-\tau_{AD}$, $D_{AD}$ may appear “high” level. As the nonlinear PD is applied, two cases can occur during different time interval $\tau$:

Case 1: $0 < |\tau| \leq \tau_{AD}$, the injected charge $Q = I_{PD} \cdot |\tau|$.

Case 2: $\tau_{AD} < |\tau|$, the injected charge $Q = I_{PD} \cdot \tau_{AD} + (I_{PD} + I_{PAD}) \cdot (|\tau| - \tau_{AD})$, which can be approximated $(I_{PD} + I_{PAD}) \cdot |\tau|$ as $\tau_{AD}$, is very small.

Generally, the total transfer function of the PD with the current-pump circuit and the loop filter can be expressed as [8]

$$K_{PD} \cdot G_{LF}(s) = \frac{I_p}{2\pi} \cdot Z_{LF}(s)$$

where $I_p$ is the pump current of the charge-pump circuit. The impedance $Z_{LF}(s)$ is the series connection of a capacitor $C_L$ and a resistor $R_Z$ with a capacitor $C_F$ added in parallel as shown in Fig. 2. The impedance of this filter can be

$$Z_{LF}(s) = \frac{1 + s\tau_Z}{s(C_L + C_F) \cdot (1 + s\tau_F)}$$

with $\tau_Z = R_Z C_L$ and $\tau_F = R_Z (C_L^{-1} + C_F^{-1})^{-1}$. The open-loop gain of the PLL equals

$$GH(s) = \frac{I_p \cdot K_{VCO}}{N} \cdot \frac{1 + s\tau_Z}{s^2(C_L + C_F) \cdot (1 + s\tau_F)}$$

which has a crossover frequency of

$$\omega_c = \frac{I_p \cdot K_{VCO} \cdot R_Z}{N \cdot C_L}$$

The open-loop gain of this third-order PLL can be calculated in terms of the frequency $\omega$, as follows:

$$GH(s) = \frac{I_p K_{VCO}}{N} \cdot \frac{1 + j\omega \tau_Z}{\omega^2(C_L + C_F) \cdot (1 + j\omega \tau_F)}$$

and its phase margin can be determined in terms of

$$\phi(\omega) = 180^\circ + \tan^{-1}(\omega \cdot \tau_Z) - \tan^{-1}(\omega \cdot \tau_F).$$
the sake of stability, the charge-pump current becomes $k^2 \cdot I_p$ instead of $I_p$ outside the locked-in region, and the loop-filter resistor would become $R_f/k$ instead of $R_f$ while $\omega$ increases $k$ times, i.e., the loop bandwidth increases $k$ times. It may speed up the switching capability of the PLL. Once it is locked on the correct frequency, the PLL will then return to the low-noise operation.

III. CIRCUIT REALIZATION

A. Architecture

The designed frequency synthesizer integrates the proposed DAPD, the charge-pump circuit, a prescaler, and a VCO in a single CMOS chip. It is similar to the structure of a conventional integer-N frequency synthesizer, as shown in Fig. 5. By adding...
the frequency-doubling block, the output frequency can be up to 900 MHz from a 450-MHz VCO.

B. Phase Detector with DAPD and Charge-Pump Filter

A schematic diagram of the DAPD is shown in Fig. 6. The phase frequency detectors are used to compare the phase difference of both input signals. The output signal \( \phi \) of the DAPD depends on the phase difference of both input signals whether it is larger than \( \tau_{AD} \) or not. Considering the delay cells with delay \( \tau_{delay} \), which is very small but never negligible, the DAPD decides the operating bandwidth of the loop filter. When \( V_i \) leads \( V_o \), the time difference \( \tau \) is larger than \( \tau_{AD} \), and \( U_{AD} \) is “low” and \( D_{AD} \) is “high.” Otherwise, when \( V_i \) lags \( V_o \), \( \tau \) is smaller than \( \tau_{AD} \) and \( U_{AD} \) is “high” and \( D_{AD} \) is “low.” In a word, if the absolute value of the time difference \( \tau \) between input signals is larger than \( \tau_{AD} \), \( FLD \) may appear “high” level. Also, the charge-pump current becomes \( k^2I_{P0} \) and the resistor of the loop filter becomes \( R_Z/k \), i.e., \( R_{AD}/R_Z \). Until the absolute value of \( \tau \) is within \( \tau_{AD} \), \( U_{AD} \) and \( D_{AD} \) are both “high,” thus \( FLD \) is brought to “low” level, then the charge-pump current and the resistor return to \( I_{P0} \) and \( R_Z \), respectively, with a narrower bandwidth for better noise rejection. However, the delay cell is adopted according to the VCO’s noise. Assuming that the phase characteristic of the signal \( V_o \) is \( \theta_0 \pm \Delta \theta \), \( \theta_{AD} \) should be larger than \( \Delta \theta \) to make the DAPD work.

In our design, the loop bandwidth \( \omega_c \) of the PLL equals about \( 2\pi \cdot 40 \) krad/s, and the loop gain zero \( \omega_z = (1/\tau_z) \) and the loop pole \( \omega_p \) are placed on a factor of four below and above \( \omega_c \), respectively. In addition, a pump current \( I_{P0} \) of 560 \( \mu A \) is applied and the parameter \( k = 3 \) is chosen. The values of the resistors \( R_z \) and \( R_{AD} \) and the capacitors \( C_z \) and \( C_P \) are 470 \( \Omega \), 235 \( \Omega \), 33 \( nF \), and 2.2 \( nF \), respectively. The open-loop gain response is depicted in Fig. 7. Curve (a) is the characteristic of the PLL with the DAPD while the bandwidth is 120 kHz. However, the PLL will return curve (b) with the bandwidth of 40 kHz when it is near in lock. These curves give the same phase margin of approximately 60°. Thus the PLL would be usually stable.

Currently, most frequency synthesizers use phase-frequency detectors (PFDs) as their PDs. A PFD is a sequential circuit which can not only detect the phase error but also provides a frequency-sensitive signal to aid acquisition when the loop is out of lock. The drawback of some conventional PFDs is a dead zone in the phase characteristic, which generates the phase error in the output signals. To solve this problem, a dynamic CMOS PFD is adopted as shown in Fig. 8(b), which is similar to the one proposed in [10]. The PFD consists of two half-transparent registers, shown in Fig. 8(a), [9] and a NAND gate. It is triggered by the negative edge of input signals. The timing diagram of the PFD is shown in Fig. 8(c). Even though the input signals are in-phase, the glitches caused by the reset path always exist. So, extra filters are added in the DAPD to remove the effect of the glitches.

So far, the positive gain of the VCO is applied from the above discussion. However, since the gain of the VCO is negative as...
described later, $U$ and $D$ of the PD connected to the charge pump should be interchanged. The charge pump, which is based on one described in [11], is adopted. It suppresses the charge sharing from the parasitic capacitance by a pair of switched-current sources.

C. Dual-Modulus Prescaler

The dual-modulus prescaler is the high-frequency building block in the frequency synthesizer. This circuit shown in Fig. 9 divides the frequency of the VCO output signal by a factor of 32 or 33 depending on the logic value of the controlled signal mode [12]–[15]. It consists of a synchronous divide-by-4/5 counter as the first stage and an asynchronous divide-by-8 counter as the second stage. The circuits in the first stage are fully differential, while the single-ended logic circuits are used in the second stage. To reduce the supply noise, an emitter-coupled logic (ECL)-like differential logic is used in the high-speed stage [16]. In the divide-by-4/5 circuit, the DFF is a differential flip-flop. Fig. 10 shows the schematic diagram of a NAND-gate logic flip-flop. Merging the logic gates to a flip-flop saves power and increases the operating speed. The toggle flip-flops are made by true single-phase clocking (TSPC) DFFs of [12] behind a differential-to-single buffer.
This buffer is used to achieve the rail-to-rail output signal in the low-speed stage.

D. VCO

The VCO is another high-frequency building block in a frequency synthesizer. Still, an ECL-like current-mode differential pair, as shown in Fig. 11, is used as a delay cell [17], [18] to achieve high common-mode rejection in a four-stage ring oscillator. The coarse tuning of the ring-oscillator’s center frequency is achieved by the bias $V_{bpo1}$ (or through the use of a digital-to-analog converter), and a fine tuning technique is needed for the PLL voltage-control path. The gain required for the oscillator is easily determined by the ratio of M1 and M2 as the current gain. The proposed delay cell has the better noise performance because the operation of the circuit is carried out by the differential signal immune to the power-supply-injected and substrate-injected noise sources. The replica bias circuit adjusts the load over a wide range in response to a swept supply current. It insures the output swing of delay cells maintain fixed and takes a changeable bias current to cover a suitable range of different output frequencies. Bypass capacitors are also an important consideration for the replica bias and voltage reference circuits. On-chip bypass capacitors can be used to help reduce their noise contribution to the ring-oscillator delay cells.

IV. MEASUREMENT RESULTS

The synthesizer is implemented in a 0.35-$\mu$m CMOS process. The microphotograph of the fabricated frequency synthesizer is shown in Fig. 12. The loop filter is off-chip, and the output signal of the VCO is connected to a source follower. The frequency synthesizer is measured at a supply voltage of 3.3 V. The frequency of the reference signal is 14 MHz. Fig. 13 shows the measured VCO transfer function by varying the controlled voltage. The measured VCO has a monotonic frequency range of 435–485 MHz. The gain of the VCO is 32.4 MHz/V at the center frequency of 460 MHz. Fig. 14 shows the output signal spectrum (using HP8560A Spectrum Analyzer after locked) of 448 MHz with the phase noise $-99$ dBc/Hz at 100-kHz offset. By adding an external frequency doubler, however, the phase noise is $-91$ dBc/Hz at 100-kHz offset from 896-MHz carrier as shown in Fig. 15. Also, the measured waveform in the time domain is also shown in Fig. 16, and its rms and peak-to-peak jitter measured by CSA803 (Communication Signal Analyzer).
are 18.9 and 110 ps, respectively. Another important parameter is the time that the PLL takes to lock in to a new frequency when channel switches. Fig. 17 shows the switching waveforms for a frequency jump from 448 to 462 MHz from the HP53310A Modulation Domain Analyzer. Obviously, the DAPD can improve the switching speed of the PLL. The power consumption is 120 mW and the chip area is $40 \times 2.0 \text{ mm}^2$ including the pad areas.
V. Conclusion

In this paper, a PLL with the DAPD is implemented in a 0.35-μm CMOS process. The proposed DAPD can be applied to enhance the switching speed of the PLL, but maintain better noise bandwidth. When adding the DAPD in the PLL, it will control the charge pump and loop filter and still maintain the loop stability with the same phase margin as in the steady state. The prototype frequency synthesizer using this structure is also implemented at 448 MHz, and the output waveform is 99 dBc/Hz at 100-kHz offset. By adding a frequency doubler, the synthesizer can operate at 896 MHz, and the output waveform is 91 dBc/Hz at 100-kHz offset from carrier.

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References


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