Gain-Enhancement Techniques for CMOS Folded Cascode LNAs at Low-Voltage Operations

Hsieh-Hung Hsieh, Student Member, IEEE, Jih-Hsin Wang, Student Member, IEEE, and Liang-Hung Lu, Member, IEEE

Abstract—In this paper, gain-enhancement techniques suitable for folded cascode low-noise amplifiers (LNAs) at low-voltage operations are presented. By employing a forward bias and a capacitive divider at the body of the MOSFETs, the LNA circuit can operate at a reduced supply voltage while maintaining an enhanced gain due to suppression of the negative impact of the body transconductance. In addition, a $G_m$-boosting stage is introduced to further increase the LNA gain at the cost of circuit linearity. Using a standard 0.18-$\mu$m CMOS process, two folded cascode LNAs are demonstrated at the 5-GHz band based on the proposed topologies. Consuming a dc power of 1.08 mW from a 0.6-V supply voltage, the LNA with the forward-body-bias technique demonstrates a gain of 10.0 dB and a noise figure of 3.37 dB. The measured $I_{1d}$ and $I_{1P}$ are $-18$ and $-8.6$ dBm, respectively. For the LNA with a $G_m$-boosting feedback, a remarkable gain of 14.1 dB gain is achieved with a dc power of 1.68 mW.

Index Terms—Body transconductance, folded cascode, forward body bias, $G_m$ boosting, low-noise amplifiers (LNAs), low power, low voltage.

I. INTRODUCTION

The increasing demand in personal wireless communications has motivated the development of fully integrated RF frontends in a CMOS process provided by commercial foundries. With the continuous shrinking of the feature size, superior high-frequency characteristics of the active devices have been demonstrated in deep-submicrometer CMOS technologies, facilitating RF integrated circuit (RFIC) designs at multigigahertz frequencies. Limited by the reliability issues in the gate oxide, the operating voltage of the MOSFETs progressively reduces with the device scaling. However, in order to sustain required noise margin and manageable leakage current for digital circuitry, the decrease in threshold voltage is not as significant. The insufficient voltage headroom has a strong impact on the performance of RF designs implemented in a conventional circuit topology. Consequently, research on low-voltage RFICs has attracted great attention and various circuit techniques have been proposed in the past few years [1]–[3].

Being widely utilized as the first active circuit in a receiver frontend, a low-noise amplifier (LNA) is a crucial component that predetermines the sensitivity and dynamic range in a wireless communication system. In order to satisfy the requirements for low-voltage operations, circuit techniques suitable for folded cascode LNAs are presented in this study. By employing the proposed forward-body-bias and $G_m$-boosting techniques, two LNA circuits were implemented in a standard 0.18-$\mu$m CMOS technology for demonstration, exhibiting enhanced RF performance at reduced supply voltage and power consumption.

This paper is organized as follows. Section II briefly introduces the circuit topology of conventional folded cascode LNAs. Sections III and IV describe the proposed circuit techniques and the design of two CMOS LNAs for low-voltage operations. Experimental results of the fabricated circuits are presented in Section V, while concluding remarks are provided in Section VI.

II. CONVENTIONAL FOLDED CASCODE LNA

With the unparalleled advantages in terms of gain, isolation, stability, and impedance matching, a cascode stage is considered one of the most widely used topologies for the implementation of LNA circuits at multigigahertz frequencies. However, with the stacking architecture of the common-source and commonsource transistors, relatively large bias voltage is required in the LNA design, and the performance degrades significantly as the supply voltage decreases. For low-voltage applications, a folded topology was proposed for cascode LNAs [4], [5]. Fig. 1 shows a simplified circuit schematic of the folded cascode LNA where $M_1$ and $M_2$ represent the first and second gain stages, respectively. In the circuit implementation, the impedance matching at input is achieved by $L_1$ and $L_2$, while the network $L_4 - C_1$ is adopted for output matching. As the inductance $L_3$ resonates with the interstage parasitic capacitance at the frequencies of...
interest, the bias current for \( M_1 \) and \( M_2 \) is provided without introducing excessive loading to the gain stages.

Due to the absence of stacking gain stages, the operating voltage of the folded cascode LNA can be reduced by one transistor overdrive. Compared with other low-voltage LNA topologies [6]–[8], the folded cascode one possesses exclusive advantages in terms of amplifier linearity, noise figure, and bias stability. However, the inherently low gain is one of the major concerns, especially for applications where the current consumption is limited. In this study, gain-enhancement techniques are proposed for the folded cascode topology and high-gain LNAs are realized for low-voltage and low-power RF applications.

III. FOLDED CASCODE LNA WITH FORWARD BODY BIAS

A. Forward-Body-Bias Technique

For a standard CMOS process without the multiple gate–oxide option, the threshold voltage can be manipulated by the dc bias at the body terminal, adding one more degree of freedom in circuit designs. Typically, the threshold voltage of an \( n \)-channel MOSFET is given as [9]

\[
V_t = V_{th} + \gamma (\sqrt{2\phi_F} + V_{SB} - \sqrt{2\phi_F})
\]

where \( V_{SB} \) is the source-to-body voltage, \( V_{th} \) is the threshold voltage for \( V_{SB} = 0 \). \( \gamma \) is a process-dependent parameter, and \( \phi_F \) is a semiconductor parameter with a typical value in the range of 0.3–0.4 V [9]. Since a forward body bias effectively lowers the threshold voltage, the MOSFETs can operate at a reduced bias voltage while maintaining equivalent device characteristics in terms of gain, linearity, and noise figure.

It is noted that, as the forward body bias turns on the source-to-body junction of the MOSFET, a dc current flows across the junction with an exponential dependence on the body voltage, leading to additional power consumption and possibly latch-up failure. In order to prevent the excessive junction conduction, a current-limiting resistor \( R_B \) is included at the body terminal. Moreover, a capacitor \( C_B \) is inserted between the body and source terminals to suppress the negative influence from the body transconductance. Fig. 2 shows the implementation of the proposed forward-body-bias technique in a triple-well CMOS technology.

Fig. 2. Forward-body-bias technique in a triple-well CMOS process.

![Forward-body-bias technique in a triple-well CMOS process.](image)

![Forward-body-bias technique in a triple-well CMOS process.](image)

B. Proposed LNA Topology

Fig. 3 shows the schematic of the proposed folded cascode LNA including the matching networks and bias circuits. To facilitate circuit design at a reduced supply voltage, the forward-body-bias technique is adopted for both \( M_1 \) and \( M_2 \). The design consideration and circuit analysis are provided as follows.

1) Gain: For small-signal analysis, the proposed LNA is treated as a two-stage amplifier, and a simplified circuit model is illustrated in Fig. 4. In consideration of the gain and reflection coefficients at the frequency of interest, the maximum power transfer can be achieved by the conjugate matching conditions [10]

\[
Z_S = Z_{IN,1}^* \quad (2)
\]
\[
Z_{OUT,1} = Z_{IN,2}^* \quad (3)
\]
\[
Z_{OUT,2} = Z_{L,2}^* \quad (4)
\]

It is noted that, in conventional circuit implementations, the interstage node of the folded cascode LNA is considered low impedance, and the Miller effect of \( M_1 \) is insignificant. However, with reduced supply voltage and power consumption, it is no longer true, as the transconductance of the second stage \( M_2 \) is inherently low. Therefore, conjugate matching is adopted in
the circuit design to achieve maximum power transfer for enhanced gain.

In the design of LNA circuits, the gain is predetermined by the transconductance of the MOSFETs. Due to the use of the forward-body-bias technique, the transistors’ threshold voltage is effectively reduced, leading to enhanced transconductance at low-voltage operations. On the other hand, with a sufficiently large current-limiting resistor $R_B$, the body of the transistor is considered floating at RF frequencies and a small-signal voltage $v_{db}$ develops between the body and source terminals. Therefore, the influence of the body transconductance $g_{mb}$ has to be taken into account in the design of the individual gain stages.

The small-signal equivalent circuit of the common-source gain stage is shown in Fig. 5 where the gate-to-drain capacitance $C_{gd1}$ is neglected to simplify the analysis. For a floating-body MOS transistor, a small-signal voltage $v_{sd1}$ is induced by the output swing due to the voltage divider established by parasitic capacitance $C_{db1}$ and $C_{sb1}$. As the signals at the input and output are typically out of phase for a common-source stage, the small-signal current resulted from $g_{mb}$ is in the opposite direction to that from $g_{m1}$, leading to a degraded transconductance of the input stage due to the use of the forward-body-bias technique. To alleviate the negative impact of the body transconductance, a capacitor $C_{B1}$ is adopted. Based on the equivalent circuit, the effective transconductance of the input stage is given by

$$G_{m1} = \frac{I_{d1}}{V_{i1}} = \frac{g_{m1}}{g_{mb1} C_{db1} + j \omega C_{db1} (C_{sb1} + C_{B1})} \cdot \frac{Z_x + 1}{C_{db1} + (C_{sb1} + C_{B1})} \cdot Z_x + 1$$

![Fig. 5. Small-signal equivalent circuit of the common-source MOSFET with the forward-body-bias technique.](image)

Typically, conjugate matching is required at the output of the common-source stage such that the LNA gain can be maximized. At the frequencies of interest, the load impedance $Z_x$ is represented as an inductive element $j \omega L_x$, the magnitude of the effective transconductance is given in (6), shown at the bottom of this page, by neglecting the real part of $Z_x$ for simplicity. For $(C_{B1} + C_{sb1}) \gg C_{db1}$, the expression in (6) is approximated by

$$|G_{m1}| = \frac{g_{m1}}{\sqrt{1 - (\omega / \omega_x)^2}} \approx g_{m1}$$

where

$$\omega_x = \frac{1}{\sqrt{L_x C_{db1}}} \quad \text{(8)}$$

For circuit implementations, $\omega_x$ is much higher than the operating frequency and the effective transconductance is simply $g_{m1}$ as the value of $C_{B1}$ is sufficiently large.

The second stage of the folded cascode LNA is realized by a common-gate pMOS transistor and its small-signal equivalent circuit is shown in Fig. 6. Since the common-gate stage typically provides a positive voltage gain, in contrast with a common-source stage, the small-signal current resulted from $g_{m2}$ aligns with that from $g_{m2}$. However, a bypass capacitance $C_{B2}$ is still adopted for optimum gain. Based on the equivalent circuit, the voltage gain of the second stage is given by (9), shown at the bottom of this page, at the operating frequency. For conjugate matching at the drain of $M_2$, the load $Y_y$ is inductive, indicating

$$|A_{v2}| = \left| \frac{V_{o2}}{V_{i2}} \right| = \frac{\sqrt{\left( g_{m2} + g_{md2} \cdot \frac{C_{db2}}{C_{db2} + (C_{sb2} + C_{B2})} \right)^2 + \left( \frac{\omega C_{db2} (C_{sb2} + C_{B2})}{C_{db2} + (C_{sb2} + C_{B2})} \right)^2 + \left( \frac{\omega C_{db2} (C_{sb2} + C_{B2})}{C_{db2} + (C_{sb2} + C_{B2})} \right)^2}} {\sqrt{\left( g_{m2} + g_{md2} \cdot \frac{C_{db2}}{C_{db2} + (C_{sb2} + C_{B2})} \right)^2 + \left( \frac{\omega C_{db2} (C_{sb2} + C_{B2})}{C_{db2} + (C_{sb2} + C_{B2})} \right)^2 + \left( \frac{\omega C_{db2} (C_{sb2} + C_{B2})}{C_{db2} + (C_{sb2} + C_{B2})} \right)^2}}$$

![Fig. 6. Small-signal equivalent circuit of the common-gate stage.](image)
a negative value of \(\text{Im}(Y_{gs})\). Therefore, the capacitance \(C_{D2}\) is chosen such that the gain of the second stage is enhanced.

2) Linearity: By taking the short-channel effects into account, the drain current of an \(n\)-channel MOSFET is given by [9]

\[
I_D = \frac{1}{2} \cdot \frac{\mu_n C_{ox}(W/L)(V_G - V_t)^2}{1 + \theta} = \frac{k_n}{2} \cdot \frac{(V_G - V_t)^2}{1 + \theta} \cdot (V_G - V_t)
\]

(10)

where \(\theta\) is the normal field mobility degeneration factor and \(\mu_n\) is the carrier mobility. In order to investigate the circuit linearity of the folded cascode LNA, the drain current of \(M_1\) is expressed by a Taylor series truncated at the third term as

\[
i_d = c_1 v_{gs1} + c_2 v_{gs1}^2 + c_3 v_{gs1}^3
\]

(11)

while the coefficients \(c_1\) and \(c_3\) can be obtained by the derivatives as

\[
c_1 = \frac{\partial I_{D1}}{\partial V_{G1}} = \frac{k_m V_{OD1}(2 + \theta \cdot V_{OD1})}{2(1 + \theta \cdot V_{OD1})}
\]

(12)

\[
c_3 = \frac{1}{3!} \cdot \frac{\partial^3 I_{D1}}{\partial V_{G1}^3} = \frac{-k_m \theta}{2(1 + \theta \cdot V_{OD1})}
\]

(13)

Note that \(V_{OD1} = V_{G1} - V_t\) represents the overdrive voltage of \(M_1\). As indicated in [11], the input 1-dB gain compression point \(P_{in-1-dB}\) is given by

\[
P_{in-1-dB} \approx \frac{0.0725}{R_S} \left| \begin{array}{c}
c_1 \\
c_3
\end{array} \right|
= \frac{0.0725}{R_S \theta} \cdot V_{OD1} \cdot (2 + \theta V_{OD1}) \cdot (1 + \theta V_{OD1})^2
\]

(14)

where \(R_S\) is the input resistance. For a folded cascode LNA, due to the concurrent operation, the linearity is mainly determined by the first stage instead of the multiple stages in a cascaded amplifier. As a result, the expression of \(P_{in-1-dB}\) in (14) is only for the input stage, providing an estimate of the amplifier linearity in the circuit design. According to (14), \(P_{in-1-dB}\) of the LNA circuit generally increases with the overdrive voltage. Due to the use of the forward-body-bias technique and inductive source degeneration, the proposed LNA is suitable for low-voltage operations without sacrificing the circuit linearity.

3) Noise Figure: Another important specification of the LNAs is the noise figure, which is strongly influenced by the design of the input stage. For a folded cascode topology with source degeneration, noise and power matching can be achieved simultaneously. To have a better understanding on the input matching, the equivalent circuit utilized for noise analysis is shown in Fig. 7, where \(v_{ns}\) and \(Z_{ns}\) are the Thévenin’s equivalent of the source, and \(v_{nd}\) and \(Z_{nd}\) represent mean-square values of the gate-induced and channel noise currents, respectively. Conventionally, the noise currents of a MOSFET are given by [12]

\[
\frac{\sigma^2}{v_{ns}} = 4kT \delta g_{bs} \Delta f
\]

(15)

\[
\frac{\sigma^2}{v_{nd}} = 4kT \gamma (g_{mn} \Delta f)
\]

(16)

where \(\delta \) and \(\gamma \) have typical values of 4/3 and 2/3, respectively. It is noted that \(g_y\) can be expressed as [12]

\[
g_y = \frac{\omega^2 C_{gds}}{\omega^2 g_{ds}}
\]

(17)

and \(g_{ds}\) is the zero-bias drain conductance. Assuming that the effect of \(g_{ds}\) is negligible, the two-port noise parameters of the equivalent circuit can be derived. The noise resistance \(R_n\), the minimum noise factor \(F_{min}\), and the optimum source impedance \(Z_{opt,1}\) are given by [12], [13]

\[
R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_{m1}}
\]

(18)

\[
F_{min} = 1 + \frac{2\omega}{\sqrt{\gamma T}} \sqrt{\gamma \delta (1 - |\epsilon|^2)}
\]

(19)

\[
Z_{opt,1} \approx j \omega C_{gds} - j \omega L_2
\]

\[
+ \frac{\sqrt{\frac{\alpha^2 \delta}{\omega T}} (1 - |\epsilon|^2) \left(1 + \sqrt{\frac{\alpha^2 \delta |\epsilon|^2}{\omega T}} \right)^2}{\omega C_{gds} \left(1 - |\epsilon|^2 \right) \left(1 + \sqrt{\frac{\alpha^2 \delta |\epsilon|^2}{\omega T}} \right)^2}
\]

(20)

where \(\alpha = g_{m1} / g_{ds}\) and \(|\epsilon|\) is a correlation coefficient with a predicted value of 0.395 [12]. Based on the small-signal analysis, the input impedance \(Z_{IN,1}\) at the gate of \(M_1\) is approximated by

\[
Z_{IN,1} \approx j \omega L_2 + \frac{1}{j \omega C_{gds} + \frac{g_{m1} L_2}{C_{gds}}}
\]

(21)

From (20) and (21), the simultaneous power and noise matching is achieved if \(Z_{opt,1}\) is the complex conjugate of \(Z_{IN,1}\), resulting in

\[
\frac{g_{m1} L_2}{C_{gds}} = \omega^2 C_{gds} \left[ \frac{\alpha^2 \delta}{\omega T} (1 - |\epsilon|^2) \left(1 + \sqrt{\frac{\alpha^2 \delta |\epsilon|^2}{\omega T}} \right)^2 \right]
\]

(22)

By properly choosing the device parameters to satisfy (22), the input stage of the LNA exhibits a noise factor of \(F_{min}\) while
maintaining a maximum power gain and a low input return loss at the operating frequency \( \omega_0 \).

With the proposed topology for the folded cascode LNA, extra design issues have to be taken into account for the noise figure. As the forward bias turns on the source-to-body junction of the MOSFET, the shot noise associated with the current across the junction contributes to additional noise sources in the LNA operation. Furthermore, since the body terminal is connected to a forward bias voltage, the noise figure may increase due to the coupling of external noise and supply fluctuation through the body. To minimize the negative impact on the circuit performance, the resistance value of \( R_B \) has to be sufficiently large to suppress the forward junction current, while the low-pass property of the network \( R_B - C_B \) can be properly designed to reject noise injection at the operating frequency.

C. Circuit Implementation

Based on the proposed folded cascode topology, a 5.2-GHz LNA is implemented using a standard 0.18-\( \mu \)m CMOS process. To facilitate the circuit design at a reduced supply voltage of 0.6 V, the device characteristics of the MOSFET under a forward body bias are first investigated. At various values of \( V_{B1} \), the simulated junction leakage and equivalent threshold are shown in Fig. 8. With a current-limiting resistance of 12 k\( \Omega \) and \( V_{B1} \) of 0.3 V, an effective threshold voltage of 0.45 V can be achieved while maintaining a junction leakage less than 0.05 \( \mu \)A.

In the LNA design, four on-chip inductors are employed for impedance-matching purposes. It is well known that the noise figure of the LNA is strongly influenced by the quality factor of \( L_1 \), which locates in the series path at the input. On the other hand, the property of \( L_3 \) plays an important role in the LNA gain. The shunt inductor \( L_3 \) serves as an RF choke such that the small-signal current generated by \( M_1 \) is directed into the source of \( M_2 \). In practice, the LNA gain is vulnerable to the shunt path resulted from the inductor losses. Therefore, in this particular design, the inductance values and the device layout for both \( L_1 \) and \( L_3 \) are optimized for \( Q \) factors, leading to enhanced LNA performance at reduced supply voltage and power consumption.

In the circuit analysis, the capacitors \( C_{B1} \) and \( C_{B2} \) are utilized to maximize the gains of the common-source and common-gate stages, respectively. To provide useful design guidelines for the capacitance value of \( C_{B1} \), circuit simulations were performed and the effective transconductance of the input stage at the 5-GHz frequency band is illustrated in Fig. 9. From the simulation results, as \( C_{B1} \) becomes four times as large as \( C_{db} \), \( |G_{m1}| \) nearly saturates to a value of 17.5 m\( \text{A/V} \). To have sufficient margin for process variation and device mismatch, the capacitance ratio is 10 in this particular design, leading to a gain enhancement of 1.4 dB at the center frequency.

As the threshold is effectively reduced by the forward body bias, the LNA exhibits reasonable linearity at low-voltage operations. Fig. 10 shows the simulated \( P_{in-1 \, \text{dB}} \) versus the gate bias of \( M_1 \) for various values of \( V_{B1} \) with \( V_{dd2} = 0.3 \) V. The linearity increases at low gate voltage as the transistors operate in weak inversion. Therefore, the tradeoff between gain and linearity has to be taken into account in determining the bias voltage of the LNA circuit.

Due to the use of the \( RC \) network at the body terminal, the influence on the LNA noise figure is investigated by circuit simulations. Fig. 11 depicts the simulated noise figure versus the current-limiting resistances. To effectively suppress the shot noise due to the forward bias at the source-to-body junctions, the resistance values, especially for \( R_{B1} \), have to be sufficiently large. According to the simulation results, the impact on the noise figure can be minimized for \( R_{B1} \) and \( R_{B2} \) larger than 5 k\( \Omega \).

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Fig. 8. Simulated threshold voltage and leakage current versus \( R_B \).

Fig. 9. Simulated \( |G_{m1}| \) versus the capacitance ratio with \( V_{B1} = 0.3 \) V.

Fig. 10. Simulated \( P_{in-1 \, \text{dB}} \) versus \( V_{G1} \) for various values of \( V_{B1} \) with \( V_{dd2} = 0.3 \) V.
Fig. 11. Simulated noise figure versus resistance values with $V_{B1} = V_{B2} = 0.3$ V.

TABLE I

<table>
<thead>
<tr>
<th>Devices</th>
<th>Design Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
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</tr>
<tr>
<td>$M_2$</td>
<td>125 $\mu$m/0.18 $\mu$m</td>
</tr>
<tr>
<td>$L_1$</td>
<td>5.7 nH</td>
</tr>
<tr>
<td>$L_2$</td>
<td>0.8 nH</td>
</tr>
<tr>
<td>$L_3$</td>
<td>2.7 nH</td>
</tr>
<tr>
<td>$L_4$</td>
<td>3.8 nH</td>
</tr>
<tr>
<td>$C_1$</td>
<td>0.15 pF</td>
</tr>
<tr>
<td>$C_{B1}$</td>
<td>1.3 pF</td>
</tr>
<tr>
<td>$C_{B2}$</td>
<td>8.2 pF</td>
</tr>
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</tr>
<tr>
<td>$V_{B2}$</td>
<td>0.3 V</td>
</tr>
</tbody>
</table>

By taking the design considerations into account, the circuit parameters of the 5.2-GHz folded cascode LNA are tabulated in Table I.

IV. LNA WITH $G_m$-BOOSTING TECHNIQUE

A. $G_m$-Boosting Technique

Based on the proposed circuit topology, a $G_m$-boosting technique can also be incorporated in the LNA design to further increase the transconductance of the MOSFETs at low bias voltage. A conceptual illustration of the $G_m$-boosting technique [14] is shown in Fig. 12. For a common-gate MOSFET, as depicted in Fig. 12(a), the transconductance is typically specified by the small-signal circuit parameter $g_m$. By introducing an inverted replica signal with an amplitude $n$ times as large at the gate terminal, the gate-to-source voltage is increased by a factor of $(1 + n)$, as illustrated in Fig. 12(b). Consequently, the transconductance is thus boosted for enhanced circuit performance. It is noted that the replica signal can be either generated by a transformer or provided by an amplifier circuit. In this study, an inverting amplifier stage is adopted for the replica signal such that the LNA gain can be maximized at reduced supply voltage and power consumption.

Fig. 12. Transistor: (a) without and (b) with the $G_m$-boosting technique.

B. Proposed Circuit Topology

Fig. 13(a) shows the circuit schematic of the folded cascode LNA with the $G_m$-boosting technique at the common-gate stage. In order to provide an inverted replica at the gate of $M_2$, a feedback loop with an additional common-source stage $M_3$, as shown in Fig. 13(b), is employed. Assuming that the voltage gain provided by the feedback stage $M_3$ is $-A_3$, the effective transconductance of the common-gate stage becomes $g_m(1 + A_3)$. For small-signal analysis purposes, the output of $M_3$ is modeled by a simplified equivalent circuit, as depicted in Fig. 13(b), and the effective voltage gain is given by

$$A_3 \approx \frac{g_m M_2 L_5}{C_{g2}} \frac{1}{\omega^2 C_3 C_{g2}} + j \frac{R_2}{\omega L_5} \left( \frac{C_3 + C_{g2}}{\omega C_3 C_{g2}} \right).$$

$$23$$
Fig. 14. Simulated: (a) gain, (b) noise figure, and (c) $P_{\text{in}}$ vs the design parameters of the feedback stage $M_3$.

By choosing the operating frequency $\omega_0$ as

$$\omega_0 = \sqrt{\frac{C_3 + C_{g2}}{L_5 C_3 C_{g2}}}$$  \hspace{1cm} (24)

the gain for the feedback stage $M_3$ is simply

$$A_3 = -g_m R_2 \left(1 + \frac{C_{g2}}{C_3}\right).$$  \hspace{1cm} (25)

As indicated in (25), $A_3$ is governed by the transconductance of $M_3$, the load resistance, and the capacitance ratio. For low-power circuit designs, it is desirable to minimize the dc current of $M_3$. Therefore, the required gain of the feedback stage is achieved by the aspect ratio of $M_3$ and the load resistance at a specified current consumption. Once the design parameters of $M_3$ and $R_2$ are determined, the values of $C_3$ and $L_5$ are chosen such that (24) satisfies.

C. Design Considerations

By incorporating the $G_m$-boosting technique in the proposed folded cascode topology, an LNA is designed and implemented at the 5-GHz band for demonstration. In order to investigate the influence of the feedback stage on the LNA performance, circuit simulations were performed and the results are shown in Fig. 14.
For a load resistance $R_L$ of 1 kΩ, the LNA gain increases monotonically with the aspect ratio and gate bias of $M_3$ due to the enhanced effective transconductance of the common-gate stage. In addition, the noise figure of the LNA is also influenced by the feedback loop established for $G_m$ boosting. As for the linearity, the concurrent operation of the gain stages $M_1$ and $M_2$ no longer exists due to the use of the $G_m$-boosting stage. Therefore, the LNA has to be treated as a cascaded amplifier and decreases accordingly. For circuit implementations, the tradeoff between gain and linearity is essential in determining the design parameters of the feedback loop in the proposed LNA topology.

V. EXPERIMENTAL RESULTS

Using a 0.18-μm CMOS process, two folded cascode LNAs were implemented at the 5-GHz frequency band for demonstration. In this particular technology, the threshold voltage of the nMOS and pMOS transistors are approximately 0.5 V without the body effect. As for the on-chip passive components, AlCu metallization layer of 2-μm thickness is available for inductors while a metal–insulator–metal structure with oxide intermetal dielectric is utilized for capacitors. The RF performance of the fabricated circuits was characterized by on-wafer probing. Based on the circuit topology presented in Fig. 3, a folded cascode LNA is realized at a center frequency of 5.2 GHz. Fig. 17 shows a microphotograph of the fabricated circuit with a chip area of $0.85 \times 0.83 \text{ mm}^2$ including the pads. Operated at a supply voltage of 0.6 V, the LNA consumes a dc power of 1.08 mW. Since the proposed $G_m$-boosting technique is considered a positive feedback, the circuit stability is also an important issue and special care has to be taken. For given aspect ratio and gate bias of $M_3$, the simulated gain and stability factor versus the load resistance are demonstrated in Fig. 15. It is clear that, at the center frequency, the stability factor degrades as the gain of the feedback stage increases. To ensure the circuit stability ($K > 1$) at all frequencies, a load resistance of 1 kΩ is finally employed in this particular design, while the simulated $|S_{21}|$ and stability factor versus frequency are shown in Fig. 16. The circuit parameters of the $G_m$-boosted folded cascode LNA are summarized in Table II.
Fig. 20. Microphotograph of the fabricated folded cascode LNA with the $G_m$-boosting technique.

![Microphotograph of the fabricated folded cascode LNA with the $G_m$-boosting technique.](image)

Fig. 21. (a) Measured and simulated $|S_{21}|$ and noise figure. (b) $|S_{11}|$ and $|S_{22}|$ of the folded cascode LNA with the $G_m$-boosting stage.

![Diagram showing measured and simulated $|S_{21}|$ and noise figure, and $|S_{11}|$ and $S_{22}$](image)

The simulated and measured small-signal characteristics are depicted in Fig. 18, indicating a gain of 10.0 dB and a noise figure of 3.37 dB at 5.2 GHz. With the on-chip matching networks, the input and output ports are matched to 50 Ω, and the measured $|S_{11}|$ and $|S_{22}|$ are $-13.4$ and $-10.6$ dB, respectively. In addition, the large-signal behavior of the fabricated LNA is evaluated and the results are demonstrated in Fig. 19. The measured $P_{in-1dB}$ and IIP3 are $-18$ and $-8.6$ dBm, respectively.

By incorporating the proposed $G_m$-boosting stage, another folded cascode LNA is also implemented at the same frequency band. The microphotograph of the fabricated circuit is shown in Fig. 20 and the chip size measures 0.97 $\times$ 0.80 mm$^2$. Biased at a supply voltage of 0.6 V, the LNA consumes a dc power of 1.68 mW. The simulated and measured small-signal characteristics are illustrated in Fig. 21, indicating a gain of 14.1 dB and a noise figure of 3.65 dB at a center frequency of 5 GHz. On the other hand, the large-signal properties of the LNA are evaluated by its $P_{in-1dB}$ and IIP3. Fig. 22 shows the measurement results with a $P_{in-1dB}$ of $-25$ dB and an IIP3 of $-17.1$ dB. It is noted that, in the proposed LNA topology, the tradeoff between gain and linearity can be realized by adjusting the gain of the feedback stage. As the gate bias of $M_3$ sweeps from 0.56 to 0.60 V, the measured LNA performance in terms of gain, noise figure, and IIP3 are tabulated in Table III, featuring a tuning mechanism for the circuit operation. Finally, Table IV summarizes the performance of the fabricated LNAs along with results from previously published works [3]–[5] for comparison. It is clear that, with the proposed circuit techniques, enhanced LNA performance is demonstrated exclusively for low-voltage and low-power RF applications.

![Diagram showing measured $P_{in-1dB}$ and IIP3](image)

TABLE III

<table>
<thead>
<tr>
<th>LNA PERFORMANCE AT VARIOUS GATE BIAS FOR THE FEEDBACK STAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{G3}$</td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>0.56 V</td>
</tr>
<tr>
<td>0.58 V</td>
</tr>
<tr>
<td>0.60 V</td>
</tr>
</tbody>
</table>

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TABLE IV

PERFORMANCE COMPARISON OF LOW-VOLTAGE AND LOW-POWER LNAs

<table>
<thead>
<tr>
<th>Technology</th>
<th>Unit</th>
<th>This Work 18.µm CMOS</th>
<th>This Work 0.18-µm CMOS</th>
<th>[3] 0.18-µm CMOS</th>
<th>[4] 0.18-µm CMOS</th>
<th>[5] 90-nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>GHz</td>
<td>5.2</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
<td>5.5</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>V</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>1.0</td>
<td>0.7</td>
</tr>
<tr>
<td>DC Power</td>
<td>mW</td>
<td>1.08</td>
<td>1.68</td>
<td>0.9</td>
<td>22.2</td>
<td>12.5</td>
</tr>
<tr>
<td>Power Gain</td>
<td>dB</td>
<td>10.0</td>
<td>14.1</td>
<td>9.2</td>
<td>13.2</td>
<td>7.0</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>dB</td>
<td>3.37</td>
<td>3.65</td>
<td>4.5</td>
<td>2.5</td>
<td>2.88</td>
</tr>
<tr>
<td>IS1_d</td>
<td>dB</td>
<td>-13.4</td>
<td>-12.7</td>
<td>-12</td>
<td>-5.3</td>
<td>-7.1</td>
</tr>
<tr>
<td>IS2_d</td>
<td>dB</td>
<td>-10.6</td>
<td>-14.0</td>
<td>-21</td>
<td>-10.3</td>
<td>-12.3</td>
</tr>
<tr>
<td>Pm_dB</td>
<td>dBm</td>
<td>-18</td>
<td>-25</td>
<td>-27</td>
<td>-14</td>
<td>-9</td>
</tr>
<tr>
<td>IIp3</td>
<td>dBm</td>
<td>-8.6</td>
<td>-17.1</td>
<td>-16</td>
<td>-</td>
<td>-7.25</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

In this study, circuit techniques are proposed for CMOS LNA designs. By incorporating a body-bias network with a $G_m$-boosting feedback in the circuit topology, enhanced gain can be achieved for folded cascode LNAs at reduced supply voltage and power consumption. Using a 0.18-µm CMOS process, two LNAs were successfully implemented at the 5-GHz frequency band for demonstration. The proposed techniques are well suited for low-voltage and low-power RF applications at multigigahertz frequencies.

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REFERENCES


Hsieh-Hung Hsieh (S’05) was born in Taipei, Taiwan, R.O.C., in 1981. He received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 2004, and is currently working toward the Ph.D. degree in electronic engineering at National Taiwan University.

His research interests include the development of low-voltage and low-power RFICs, multiband wireless systems, RF testing, and monolithic microwave integrated circuit (MMIC) designs.

Jih-Hsin Wang (S’06) was born in Taipei, Taiwan, R.O.C., in 1984. He received the B.S. degree in electronic engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2006. Currently, he is working toward the master degree in electronic engineering at National Taiwan University, Taipei, Taiwan, R.O.C. His research interests include the development of low-voltage and low-power RFICs.

Liang-Hung Lu (M’02) was born in Taipei, Taiwan, R.O.C., in 1968. He received the B.S. and M.S. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1991 and 1993, respectively, and the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 2001.

During his graduate study, he was involved in SiGe HBT technology and MMIC designs. From 2001 to 2002, he was with IBM, where he was involved with low-power and RFICs for silicon-on-insulator (SOI) technology. In August 2002, he joined the faculty of the Graduate Institute of Electronics Engineering and the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C., where he is currently an Associate Professor. His research interests include CMOS/BiCMOS RF and mixed-signal integrated-circuit designs.