Amorphous ZnO transparent thin-film transistors fabricated by fully lithographic and etching processes

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Oxide-semiconductor-based thin-film transistors (TFTs), particularly the amorphous ones, are becoming an important emerging technology. Since oxide semiconductors easily form polycrystalline phases, usually more complicated oxide mixtures are needed for growing amorphous phases. In this letter, we report that by simply reducing the thickness, ZnO can be intentionally grown into the amorphous phase. Furthermore, both top-gate and bottom-gate amorphous ZnO TFTs of micrometer scales were effectively implemented using fully lithographic and etching processes. Rather high field-effect mobilities of 25 and 4 cm²/V s and on/off current ratios of >10⁷ and >10⁶ were achieved for top-gate and bottom-gate configurations, respectively. © 2007 American Institute of Physics. [DOI: 10.1063/1.2753724]

Oxide-semiconductor-based thin-film transistors (TFTs) have advanced remarkably in recent years, and provide an attractive alternative to silicon-based or organic TFTs.1–3 Oxide semiconductors composed of heavy-metal cations with (n−1)dz⁰ns⁰ (n ≥ 4) electronic configurations are usually wide bandgap and transparent materials,4–9 making transparent electronics and very high-resolution displays (e.g., high aperture ratios) possible. Furthermore, spherically symmetrical ns orbitals have large radii and large overlap between adjacent orbitals, thus giving an efficient transport path for carriers and high carrier mobilities. In addition, such orbital overlap is rather insensitive to the degree of disorder in films, rendering possible high mobilities even in the amorphous phase. Compared to polycrystalline ones, amorphous oxide semiconductors could have lower processing temperatures (thus better compatibility with flexible substrates), better uniformity and sometimes even higher carrier mobilities due to lack of grain-boundary issues.

Among various oxide semiconductors, ZnO-based materials are one of the most studied systems, partly because of richer Zn-based minerals on earth and thus potentially lower cost (e.g., compared to In-based materials). Since ZnO easily forms polycrystalline phases even at room temperature, amorphous ZnO-based semiconductors (e.g., In–Zn–O, Zn–Sn–O, In–Ga–Zn–O, In–Al–Zn–O, etc.) are usually grown by mixing several metal oxides to prevent crystallization.4–9 In this letter, without mixing oxides (thus simpler compositions), we show that by simply reducing the thickness, ZnO can be intentionally grown into the amorphous phase. Furthermore, due to lack of high-selectivity etching techniques for oxide semiconductors and transparent oxide conductors (e.g., indium tin oxide, ITO), previously reported transparent TFTs (TFTTs) were mostly fabricated by shadow-masking or lift-off techniques.8–9 In this work, both miniaturized top-gate and bottom-gate amorphous ZnO TFTTs with rather high mobilities had been effectively implemented using fully lithographic and etching processes.

Figures 1(a) and 1(b) show the schematic structures of the top-gate and bottom-gate ZnO TFTTs studied, respectively. For top-gate TFTTs, patterned ITO (120 nm) on glass substrates was used as the source/drain electrodes. The ZnO layer of various thicknesses was deposited by rf sputtering in Ar/O₂ without intentional heating. 50 nm SiNₓ was then deposited by plasma enhanced chemical vapor deposition (PECVD) at 200 °C as the etching mask and the passivation layer for ZnO since it can be easily damaged or degraded by chemicals used/produced during lithography.10–12 To ensure the temperature uniformity, the SiNₓ deposition was started 20 min after the substrate temperature reaching 200 °C. This SiNₓ layer was first patterned by lithography and reactive ion etching (RIE) and then was used as the hard mask for patterning ZnO. The etchant used for patterning ZnO must be carefully chosen since many etchants for ZnO also etch ITO. In this work, it was found that some weak acids and bases possess high etching selectivity between ZnO and ITO, rendering microfabrication of TFTTs more feasible. Subsequently, another 150 nm SiNₓ was deposited by PECVD at 200 °C to complete the gate insulator stack, followed by the deposition and patterning of the 120 nm ITO gate electrode. Finally, the gate insulator was etched by RIE to expose source/drain contacts. For the bottom-gate ZnO TFTTs (also with 200 nm SiNₓ as the gate insulator), all layers were processed using the same conditions, except for the difference in the process sequence. In both types of TFTTs, the channel width (W, 100 μm) and the channel length (L, 10 μm) were

![FIG. 1. Device structures of (a) top-gate and (b) bottom-gate ZnO TFTTs.](image-url)
defined by the ITO source/drain patterns, and no postfabrication annealing (in addition to heating at 200 °C for SiNₓ growth) was performed. Both TTFTs together with the glass substrates show high transmittance of >80% over the whole visible range (400–700 nm).

Figure 2(a) shows the x-ray diffraction (XRD) patterns of room-temperature sputtered and 200 °C annealed (to mimic deposition of SiNₓ) ZnO films with different thicknesses on glass substrates. For ZnO films thicker than 40 nm, a dominant peak at 2θ = 34.4° that corresponds to the (002) orientation of the ZnO wurtzite (hexagonal) structure is observed, indicating formation of polycrystalline ZnO and preferential orientation of the c axes along the surface normal. Interestingly, for ZnO films with thicknesses of 20 and 10 nm, no x-ray peaks could be detected. Similarly, thin ZnO films (e.g., 10 nm) grown on top of the amorphous SiNₓ also reveal no crystallization peaks [Fig. 2(b)]. A further check of the topology and morphology of thin films by atomic force microscopy (AFM) and scanning electron microscopy (SEM) also reveals very different features for thick and thin ZnO films. Figures 3(a) and 3(b) show the AFM phase images (which distinguish nanoscale features better than height images) of the 10 and 60 nm ZnO films on glass substrates, respectively. Figures 3(c) and 3(d) show SEM images of the same two samples. In both AFM and SEM images, while hardly any grains are distinguishable for the 10 nm ZnO film (indeed both AFM and SEM images are simply similar to those of a glass substrate), grains of tens of nanometers are clearly visible for the 60 nm ZnO film.

In Fig. 4, the root-mean-square (rms) roughnesses and the average grain sizes derived from the AFM or SEM images of ZnO films on glass substrates are shown as a function of the ZnO thickness, which further manifest the thickness-dependent morphologies. Both the roughness and the grain size show an evident increase for films thicker than 40 nm, but a negligible change below 20 nm. All the results of Figs. 2–4 indicate a transition from the amorphous to the polycrystalline structure with increasing the ZnO thickness. The amorphous morphology of thin ZnO films (either on the glass or SiNₓ) is not associated with the shorter deposition or annealing time, since with much more extended annealing (e.g., at 200 °C for 6 h), thin ZnO films remain amorphous. Previously, similar thickness dependence of crystallinity had also been observed for various materials. During thin-film deposition, a new coming particle in general would have a high tendency to relax in the same phase of nearby particles. Therefore in the initial stage of growth, nucleation of ZnO nanocrystallites may be suppressed at/near the interface to the amorphous substrate (either glass or SiNₓ), giving an amorphous structure. As the thickness increases, the crystallites (now away from the amorphous substrate) would have larger freedom to coalesce, resulting in larger grains and crystalline phases. In the present work, by decreasing the thickness of the ZnO film below some tens of nanometers, smooth amorphous and grain-boundary-free ZnO films are obtained.

Figure 5 shows the output characteristics (drain current I_D as a function of the drain-to-source voltage V_DS, under different gate biases V_GS) of a top-gate TTFT with 60 nm ZnO, a top-gate TTFT with 10 nm ZnO, and a bottom-gate TTFT with 10 nm ZnO (all with W/L = 100 μm/10 μm). Although all three devices were processed in similar conditions, the TTFT with 60 nm ZnO neither turns on nor shows transistor characteristics, yet both TTFTs with 10 nm ZnO show typical transistor characteristics in the n-type enhancement mode. Considering the polycrystalline and amorphous characteristics of the 60 and 10 nm ZnO, respectively, it is most possible that the present device processing conditions (with processing temperatures only up to 200 °C) is not suf-
sufficient to activate the polycrystalline ZnO (e.g., annealing the grain-boundary defects, etc.) for TFT operation. In contrast, since there are no grain boundaries in the thin and amorphous ZnO, the as-fabricated TTFTs readily show well-behaved transistor operation. For the 10 nm ZnO TTFT, it is also seen that the top-gate TTFT shows much larger drain currents than the bottom-gate TTFT. The difference between these two configurations may be associated with two factors. First, from our AFM results, the rms roughness of the 10 nm ZnO on SiN/ITO/glass (bottom-gate case) is 4.26 nm. The larger roughness of the channel and the channel/dielectric interface could degrade the carrier transport.16,17 Second, in bottom-gate TTFTs, the surface of the SiN gate insulator had been exposed to multiple processing steps before ZnO deposition, which may degrade the channel/dielectric interface property. In contrast, for top-gate TTFTs, the SiN was deposited right after ZnO, leaving the interface intact.

Figure 6 shows transfer characteristics [Fig. 6(a): $\log(I_D)$ vs $V_{DS}$ for $V_{GS}=10.1$ V, Fig. 6(b): $I_D$ vs $V_{GS}$ in the saturation mode for $V_{DS}=10.1$ V] of the top-gate and bottom-gate TTFTs with 10 nm ZnO. It is also seen that the gate leakage currents in both TTFTs are as low as $10^{-12}$ A. From Fig. 6(b), the saturation mobility $\mu$ and the threshold voltage $V_t$ are extracted using the saturation current equation of a field-effect transistor, $I_D=(1/2)\mu C_i(W/L)(V_{GS}-V_t)^2$, where $C_i$ is the capacitance per unit area of the gate insulator. A high mobility $\mu \sim 25$ cm$^2$/V s and a $V_t \sim 4.53$ V are extracted for top-gate TTFTs, while $\mu \sim 4$ cm$^2$/V s and $V_t \sim 2.63$ V are obtained for bottom-gate TTFTs. From Fig. 6(a), the subthreshold slopes and the on/off current ratios are estimated to be $(1.24$ V/decade, $2.3 \times 10^5$) and $(1.82$ V/decade, $1.4 \times 10^6$) for the top-gate and bottom-gate TTFTs, respectively. Comparison of device characteristics indicates significant influences of the device structures and processing sequences on TTFT performances.

In summary, we show that by simply reducing the film thickness, ZnO can be intentionally grown into the amorphous phase, providing a simple and effective approach for growing amorphous oxide semiconductors. Furthermore, both miniaturized top-gate and bottom-gate amorphous ZnO TTFTs with rather high mobilities had been effectively implemented using fully lithographic and etching processes. These developments shall be useful to further advance the TTFT technology for real applications.